A CAHNERS PUBLICATION INTERNATIONAL EDITION AUGUST 21, 1986

EDN

SPECIAL ISSUE:
Military electronics

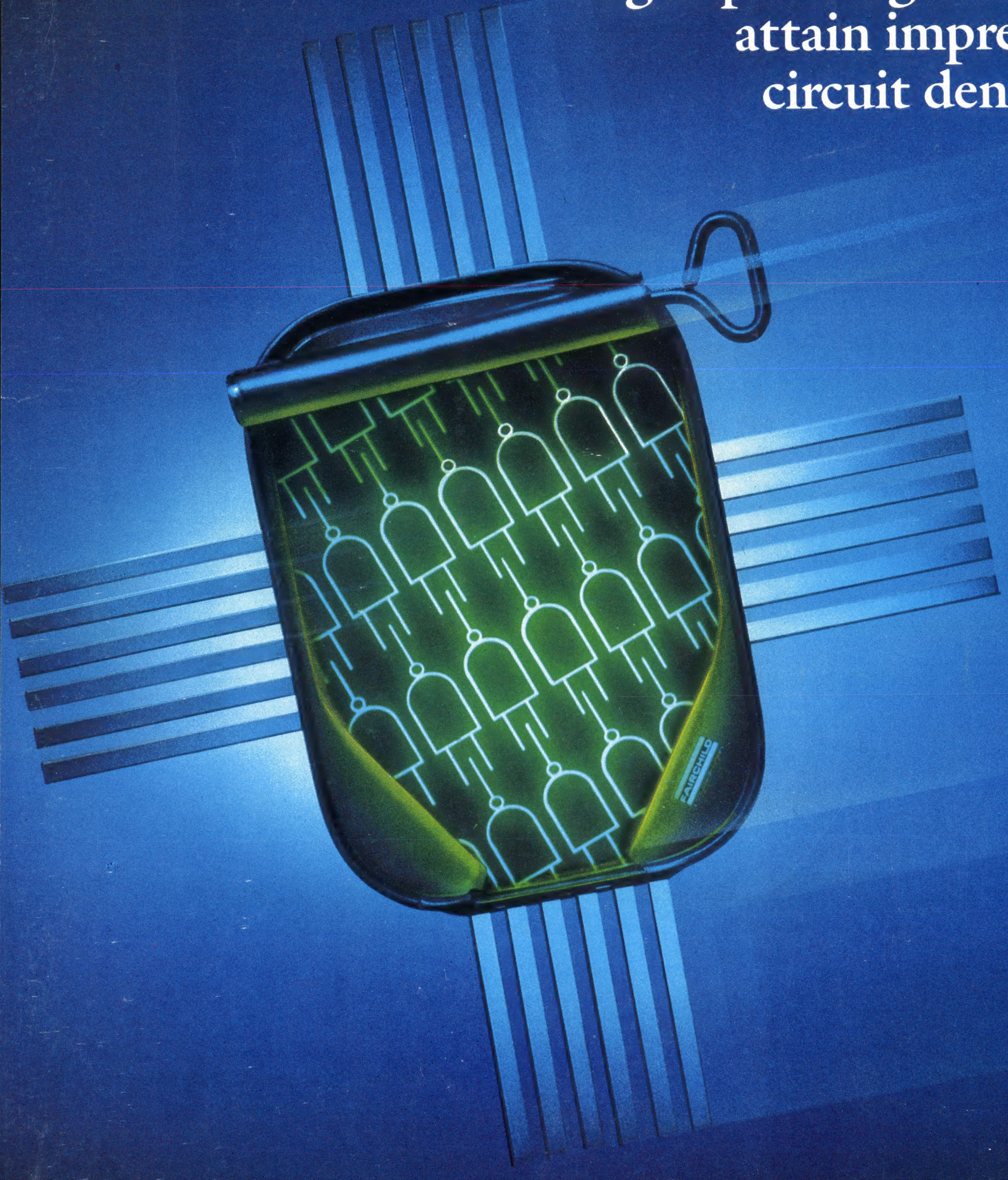
Rad-hard CMOS devices suit low-power satellite systems

Precision components yield effective EW radar

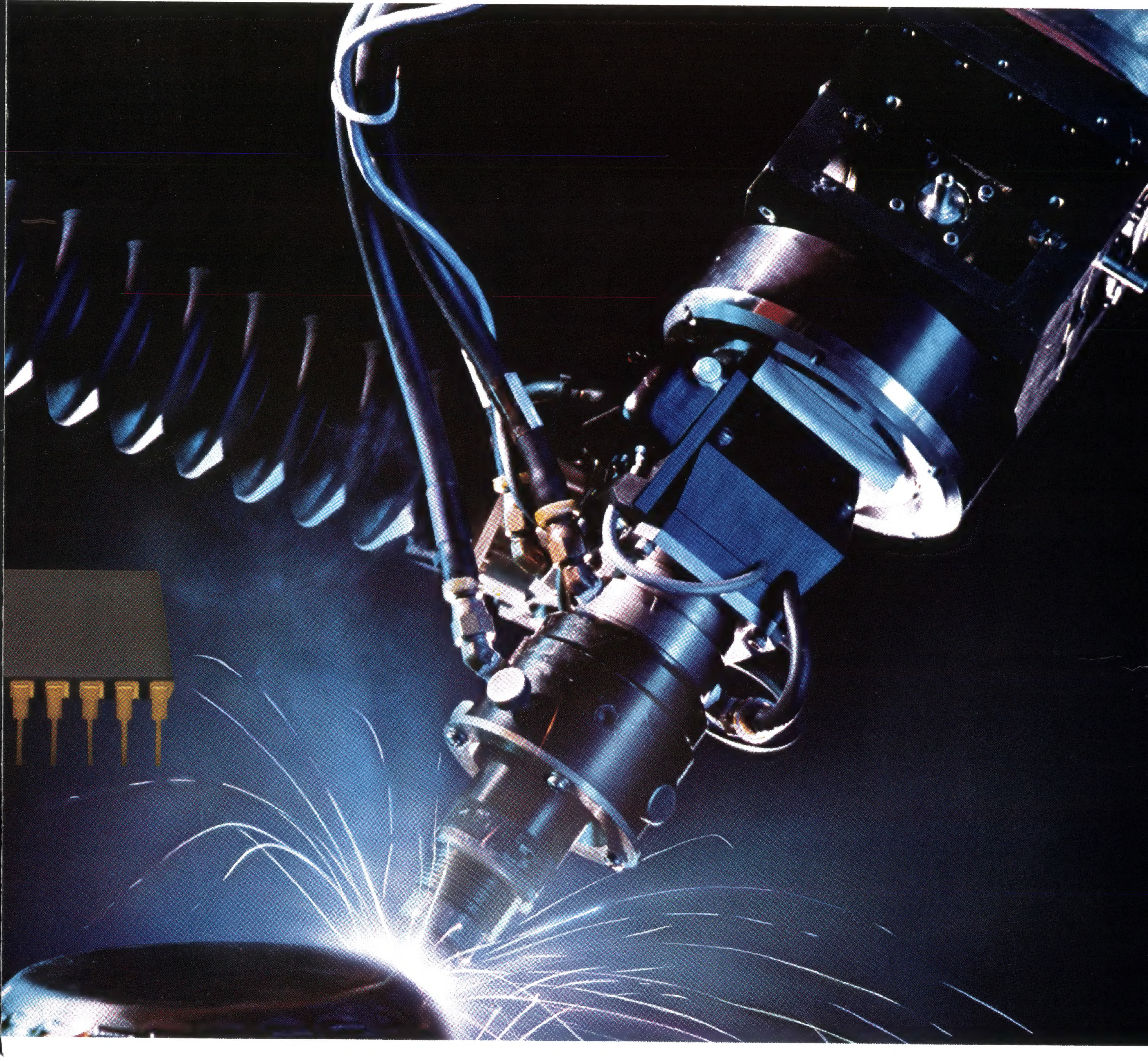
Characterizing GaAs chips

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEE

High-speed digital chips attain impressive circuit densities



stands alone.



error correction technique, the ICL7134 provides up to 14 bits of accuracy and ultra-high stability over the entire operating temperature range. Plus the same cool low-power CMOS performance.

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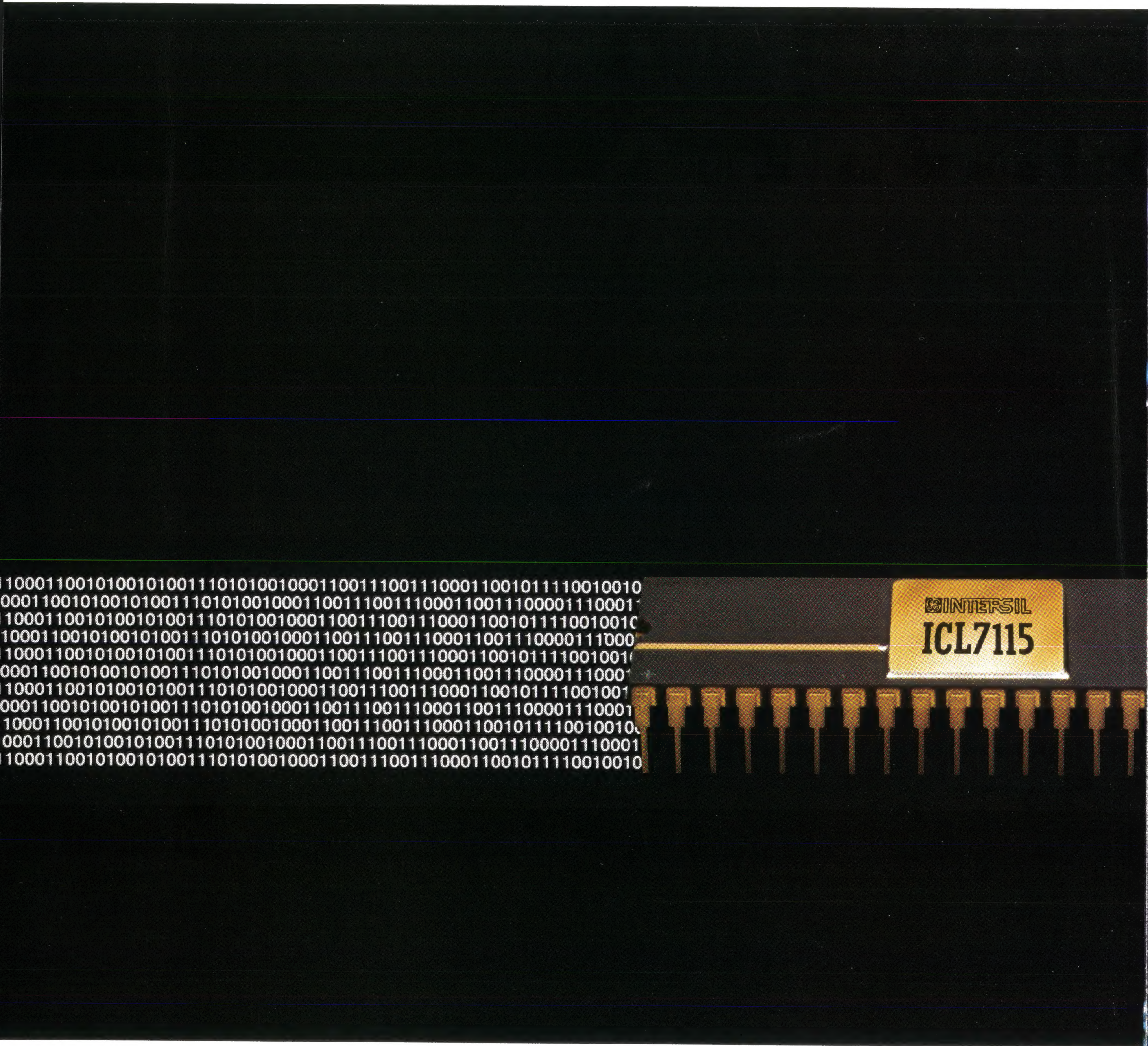

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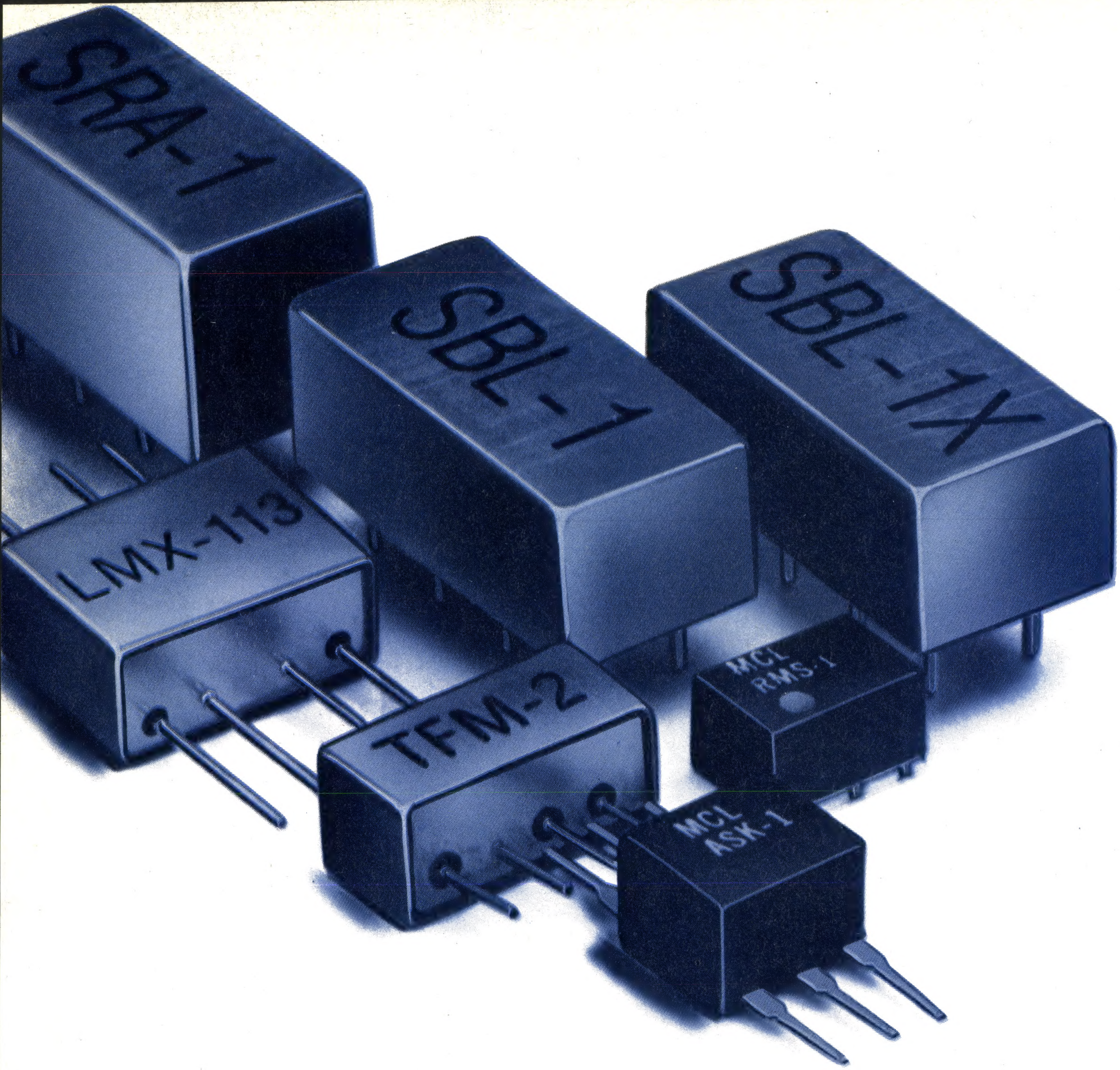

more tough mixers

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*units are not QPL listed
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LOW PASS Model *LP–	10.7	50	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to	10.7	48	98	140	190	270	400	520	580	700	780	900
Max. 20dB Stop Frequency (MHz)	19	70	147	210	290	410	580	750	840	1000	1100	1340

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HIGH PASS Model *HP–		50	100	150	200	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.	41	90	133	185	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	190	290	365	460	520	570	660	720

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* Prefix P for pins, B for BNC, N for Type N, S for SMA *example:* **PLP-10.7**

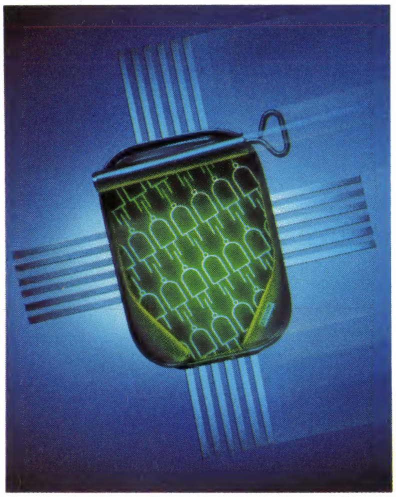
C105 REV. A

Volume 31, Number 17

EDN

August 21, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** Manufacturers that squeeze out interconnect delays by packing dense high-speed circuitry into their glue-logic packages are taking one approach to meeting the needs of commercial datacomm, telecomm, and supercomputer applications and the military's VHSIC and various DARPA projects. See pg 112. (Photo by Imagination; courtesy Fairchild)*

SPECIAL ISSUE: MILITARY ELECTRONICS

DESIGN FEATURES

Special Report: High-speed logic ICs 112

High-speed glue logic plays an obvious role in a world of ever-increasing computing power, and GaAs, ECL, and CMOS remain the dominant technologies for these high-speed logic ICs. Each can claim niches in which their respective advantages prove best, but process developments will continue to create areas of competition.
—Denny Cormier, Regional Editor

Examine and verify GaAs IC performance 127

By applying appropriate input signals, employing a sampling scope, and using certain techniques, you can measure the propagation delays and setup and hold times of GaAs chips and corroborate your vendor's specs.*—Louis Pengue, TriQuint Semiconductor, and Eldon Walters, Tektronix*

Design low-power, rad-hardened satellite systems 145

Satellite systems have two major design requirements: They must be radiation hardened, and they must operate on low power. To design such systems, you must use careful shielding, grounding, and decoupling techniques, and you must incorporate low-power, rad-hardened devices, such as rad-hardened CMOS arrays, in your systems.
—Bob Pearson, Harris Semiconductor

Precision components let you build effective EW radars 157

To protect radar transmitters from power losses, spurious emissions, and other irregularities that lower performance, use precision transmitter microwave components and careful design techniques.
—John McCrea and Charlie Schumann, Waveline Inc

Use CMOS DACs to generate sine waves 167

You can use microprocessors in combination with D/A converters to generate sinusoidal waveforms with controllable and repeatable characteristics. One technique uses EPROM look-up tables to store sine-wave values; another method treats D/A converters as microprocessor-controlled potentiometers in a classical, active RC-oscillator circuit.*—John Wynne and Mike Byrne, Analog Devices Semiconductor*

Continued on page 7

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Continued from page 5

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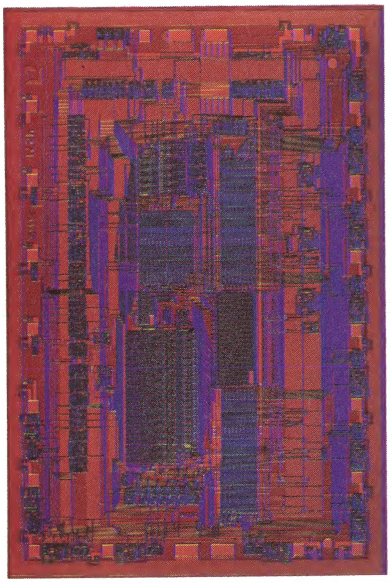

***Frequency-manipulating ICs** that employ phase-locked-loop and variable-modulus-divider schemes can now handle higher frequencies than their predecessors could. Innovative devices range from a programmable event generator that achieves 10-nsec resolution to a 2-GHz GaAs chip that's useful in UHF synthesizer applications (pg 53).*

TECHNOLOGY UPDATE

Phase-locked loops and frequency dividers handle higher-speed circuit functions 53

Several recently introduced frequency-manipulating ICs use phase-locked loops and digital counter (divider) circuitry to achieve a variety of results — for example, FM demodulation, and frequency division and multiplication. The new ICs handle higher frequencies than their predecessors, and some now employ gallium arsenide technology.
—Bill Travis, Senior Editor

Multiprocessor computers execute tasks in parallel for faster performance 75

It's been 14 years since the University of Illinois developed the first massively parallel computer (Illiac IV) and had it installed at NASA's Jet Propulsion Labs. Research into the hardware and software problems of parallel processing has continued at all levels, and it's now possible to link inexpensive processors to yield the performance of a supercomputer at a fraction of the cost of an equivalent uniprocessor.*—Chris Terry, Associate Editor*

PRODUCT UPDATE

D/A-converter IC 89
PC-based board and VAX link 91

DESIGN IDEAS

Circuit provides controllable resistance 183
PLD provides chip select and wait states 184
High-gain amp yields low dc output offset 186
Z80 μP system utilizes an 8259 PIC 188
Subroutines handle speech companding 191

Continued on page 9

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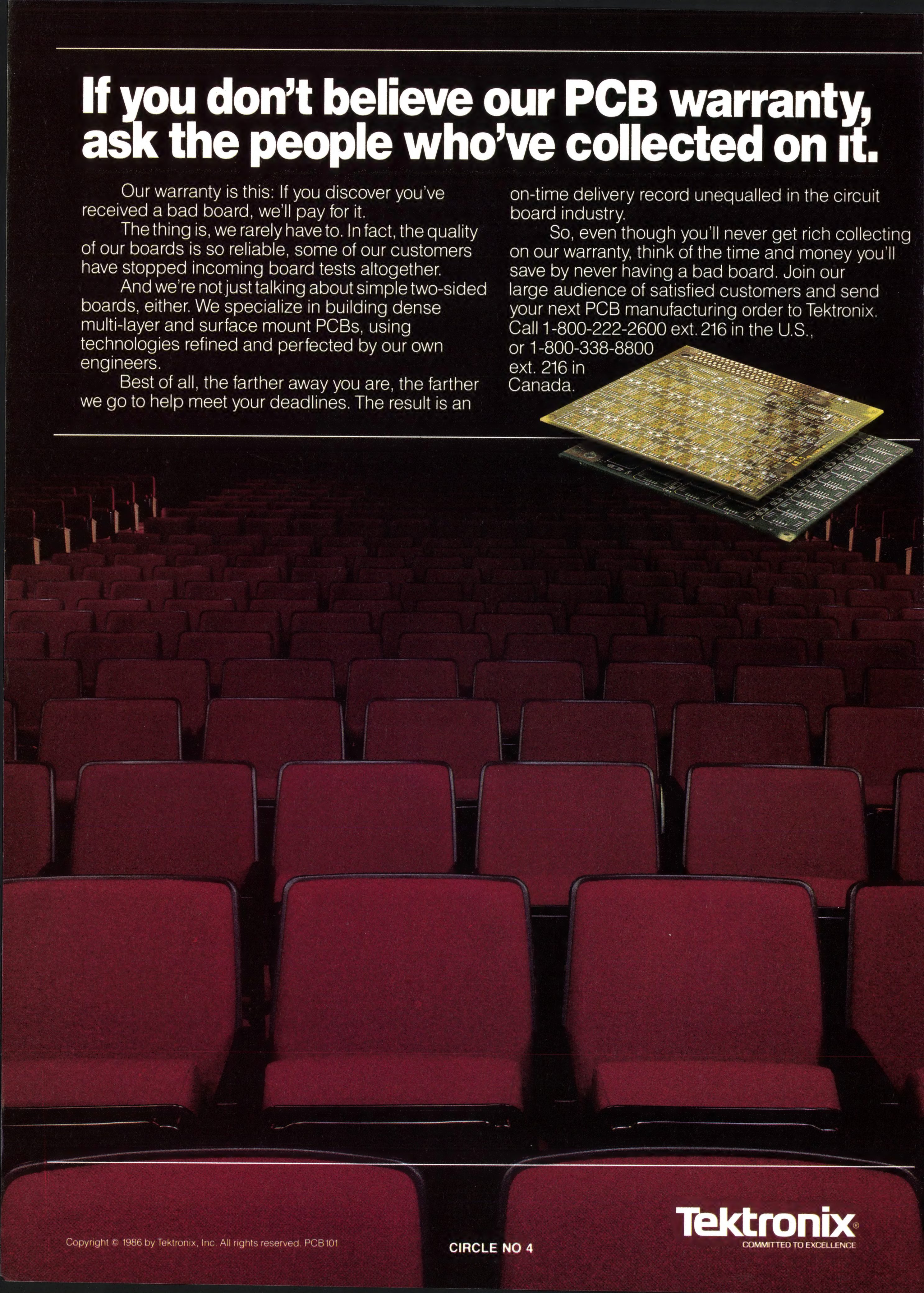

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CIRCLE NO 4

Continued from page 7

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August 21, 1986

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Rick Nelson
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Home Office Editorial Staff
275 Washington St, Newton, MA 02158
(617) 964-3030
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San Diego, CA: (619) 748-6785
Peter Harold, *European Editor*
0603-630782
(St Francis House, Queens Rd,
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EDITORIAL 47

As parallel processors increasingly find use in engineering applications, you'll have to struggle to keep up with the machines' capabilities.

NEW PRODUCTS

Computer-Aided Engineering 200
Computers & Peripherals 206
Components & Packaging 217
ICs & Semiconductors 226
Computer-System Subassemblies 232
Instrumentation & Power Sources 240
International 248
Software 252

PROFESSIONAL ISSUES

Consulting engineers pay a high price while fighting for liability law reform.—*Deborah Asbrand, Staff Editor* 275

When Stanford recruits for its MSEE program, the name of the game is personal attention.—*Deborah Asbrand, Staff Editor* 278

LOOKING AHEAD 307

Semicustom linear IC market to be worth $360M by 1990. . . Datacomm systems to use $1B of F-O equipment by 1995.

DEPARTMENTS

News Breaks 19
News Breaks International 22
Signals & Noise 30
Calendar 38
Readers' Choice 96
Leadtime Index 109
Literature 262
Business/Corporate Staff 268
Market Forecast 270
New Books 272
Career Opportunities 280
Advertisers Index 305

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The technology of the future is recording data today.

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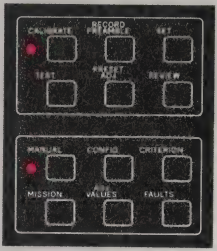
It's the only recorder with a transport that combines double vacuum buffering with a dual capstan drive system. This technology provides incredibly gentle tape handling and minimizes mechanically-induced artifacts with a 1000 Hz servo bandwidth for maximum flutter rejection and minimum TBE.



Auto calibration and test panel

The Model 97 has a computer-controlled feature set that includes:

- Direct electronics to 4.0 MHz, FM to 1 MHz and serial digital to 8 Mbps per track
- Integral time code generator/reader/search and control system
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The solid-ferrite heads of the Model 97 are so dependable that they're warranted for 5 years or 200 million feet of tape.

The Model 97 data system also has fully automatic calibration and test of its record and reproduce electronics. This eliminates the potential loss of data due to faulty manual calibration and setup.

The future is yours with the Model 97. For more information, contact Ed Haines, Honeywell Test Instruments Division, Box 5227, Denver, CO 80217. (303) 773-4834.

Together, we can find the answers.

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If your system is only using this many colors, isn't it time to grow up?

The INMOS IMSG170 Color Look-up Table offers a grown-up solution to video display color enhancements. It lets you and your RGB analog display advance to a palette of more than a quarter million colors.

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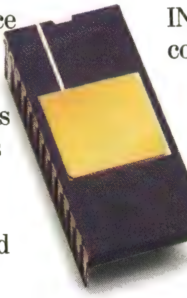

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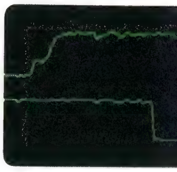
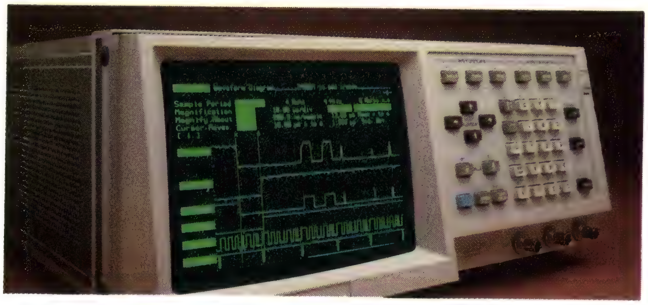


The HP 1631 A/D.



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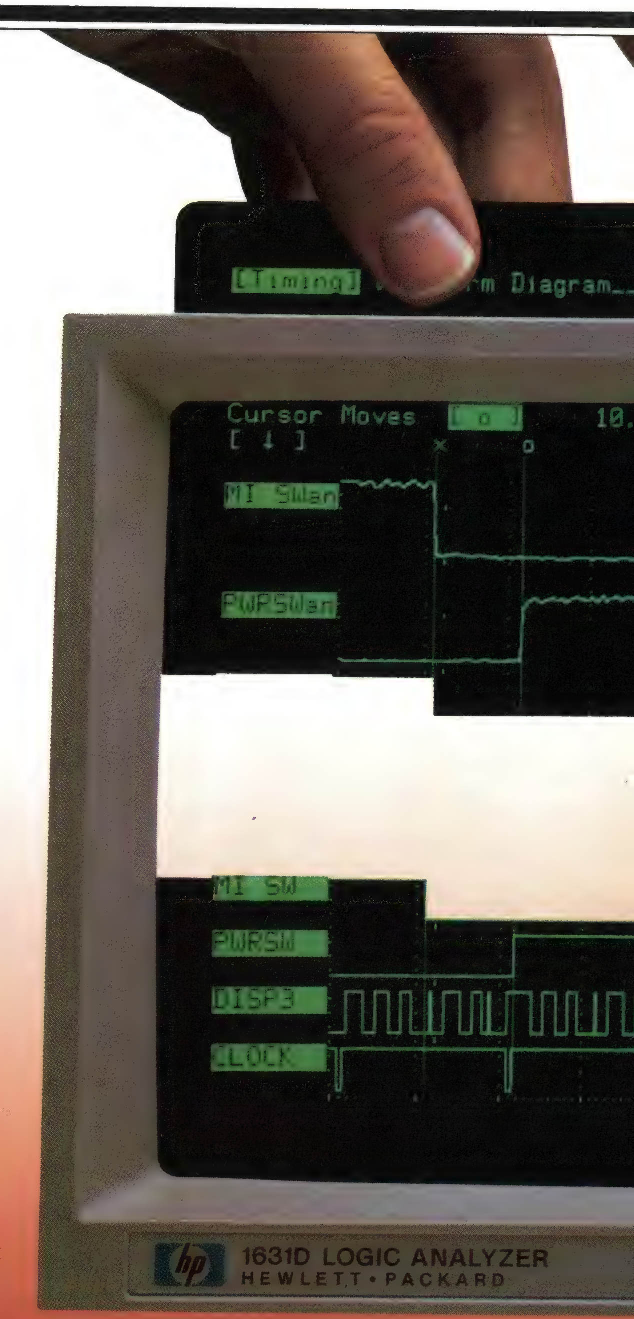

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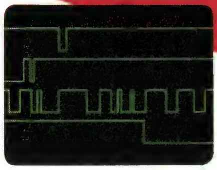

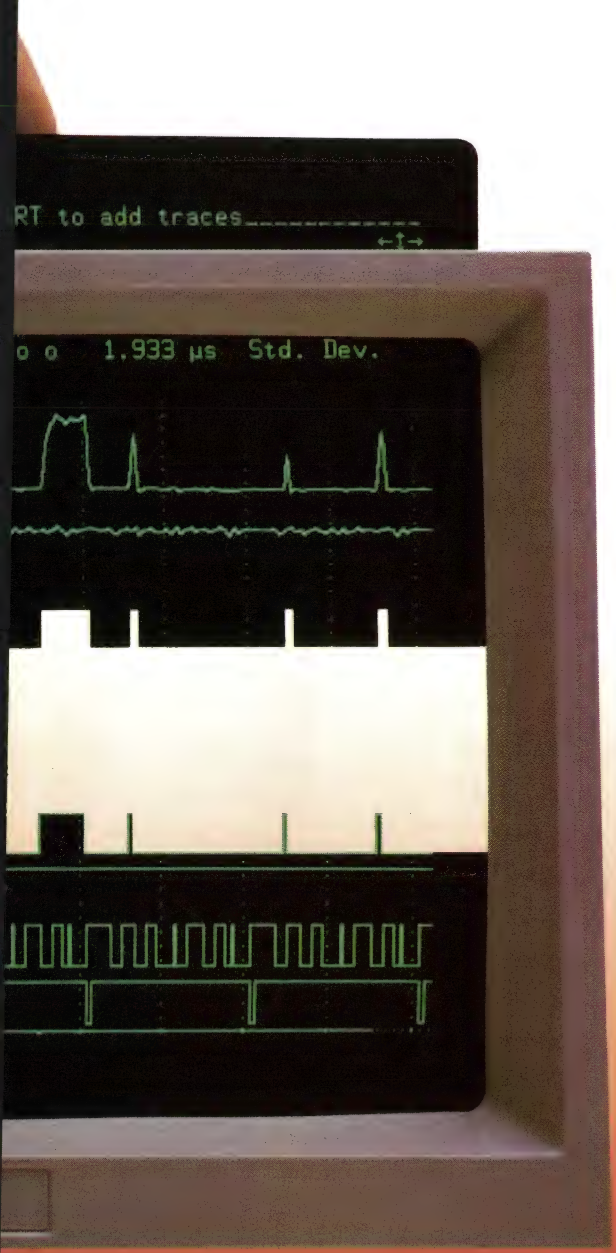

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CIRCLE NO 13

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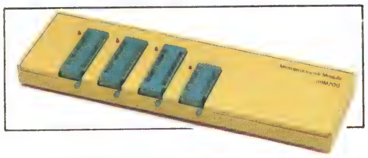

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CIRCLE NO 15

NEWS BREAKS

EDITED BY JOAN MORROW

HIGH-SPEED ICs RECEIVE NEW PACKAGING, SECOND SOURCING

Because of noise generated by interpin coupling within CMOS glue-logic DIP ICs at frequencies higher than 100 MHz, Texas Instruments (Dallas, TX, (800) 232-3200) and Signetics/Philips (Santa Clara, CA, (408) 991-3627) will not offer their alternate-sourced families of 54/74 Advanced CMOS Logic (ACL) chips in standard JEDEC DIPs having conventional pinout configurations. Instead, to remedy the noise problem, both companies are converting the footprints on their own high-speed ACL glue-logic parts to a newly proposed JEDEC DIP-pinout standard.

This proposed packaging standard relocates all inputs to either side of the V_{CC} pins and all outputs to either side of the ground pins. In addition, all input and output pins are kept on opposite sides of the package. These changes permit low-noise operation, with full 24mA output drive current at clock frequencies as high as 200 MHz.

In another development involving high-speed CMOS logic ICs, Hitachi America Ltd (San Jose, CA, (408) 435-8300) will second-source Fairchild Semiconductor Corp's (Cupertino, CA, (408) 864-6250) Advanced CMOS Technology (FACT) family of 54/74 high-speed glue-logic ICs. By using its 1.2-μm silicon-gate process, Fairchild has held power consumption of FACT devices to 0.1 mW/gate while still maintaining 1-nsec gate delays. Some members of the FACT family can run at 200-MHz clock speeds.

Hitachi is already shipping 10 FACT parts, and another 10 will be available in the fourth quarter. A total of 120 FACT glue-logic devices are planned for alternate-sourcing by the two companies in the second half of 1986. The Fairchild/Hitachi agreement also meets DoD's DESC second-sourcing requirements. (For a detailed report on high-speed logic ICs, turn to pg 112).—Denny Cormier

ON-LINE DATABASE PROVIDES IC AND COMPONENT INFORMATION

You can access the DesignLine on-line engineering database from ANSI terminals or from personal computers with communications software. Available from Engineering Information Services (EIS) (Cupertino, CA, (408) 255-4900), the database contains product descriptions and performance specifications for integrated circuits and discrete semiconductor components from most major suppliers. By running free software provided by EIS, IBM PCs and compatibles can retrieve both text and graphics information. Connect time costs $60 per hour. EIS claims to have 60 product catalogs in its database and expects to add 60 more by the end of the year.—Gary Legg

PROGRAMMABLE LOGIC DEVICE FEATURES IN-CIRCUIT PROGRAMMING

An on-chip shift register and a 5V programmable, electrically erasable fuse array allow you to program, erase, and reprogram a Lattice Semiconductor (Beaverton, OR, (503) 629-2131) ispGAL 16Z8 while it is installed in-circuit on your pc board. Although not pin compatible because of its 24-pin, 0.300-in.-wide package, the $15 (1000) 16Z8 can emulate 21 members of Monolithic Memories' 20-pin PAL family through both function and fuse-map compatibility. It's available in 25- and 35-nsec versions.

The extra four pins on the 16Z8 are connected to an internal shift register's input, output, clock, and mode-control signals. You can use the shift register to program the fuse map in the 16Z8; you can also use the shift register as a serial-scan-path register for creating serial diagnostic loops in your designs. The fuse array, which is rated for a minimum of 10,000 erase/write cycles and which includes a program-security feature, is tested at the factory, allowing the company to guarantee 100% field programmability of the parts.—Steven H Leibson

NEWS BREAKS

SINGLE-CHIP MODEM MEETS THREE COMMUNICATION STANDARDS

Providing full-duplex operation on a single chip, the TSG7515 from Thomson-Mostek Corp (Carrollton, TX, (214) 466-6178) is a CMOS modem that meets the Bell 212A, Bell 103, and CCITT V22 A/B communication standards. By selecting different pins, you can alter the IC's operating mode and achieve data rates from 300 to 1200 bps. The TSG7515 can generate and receive both phase- and frequency-modulated signals. During operations involving phase modulation, the IC's data buffer lets it handle both asynchronous and synchronous data streams. The chip contains a 4.9152-MHz crystal for frequency reference; a built-in scrambler ensures that the modem transmits a continuously changing pattern. The $53.80 (100) TSG7515 typically consumes 100 mW from a ±5V power source.—J D Mosley

AC ANALYSIS PROGRAM CALCULATES DEVICE CHARACTERISTICS

Hewlett-Packard Co (Palo Alto, CA) has added an ac analysis package to its Transistor Electrical Characterization and Analysis Program (TECAP). TECAP is used to collect measured data from a semiconductor device, calculate its dc model parameters, and run a Spice simulation to compare the model's operating characteristics with the device's operating characteristics. With the $15,000 package, you don't have to rely on the dc model parameters to characterize a high-frequency device. TECAP measures all S, H, Y, and Z parameters using Hewlett-Packard's network analyzers and extracts the ac model parameters needed to obtain device resistance, capacitance, and transit-time information. Then TECAP can directly compare the Spice results to the measured high-frequency behavior of high-speed bipolar, gallium-arsenide, and monolithic microwave integrated-circuit devices.—Chris Everett

MONOLITHIC DIGITAL TIMING IC OFFERS 10-nSEC PRECISION

You can use the Am2971 programmable event generator from Advanced Micro Devices (Sunnyvale, CA, (408) 732-2400) to gain 10-nsec timing precision in your circuit or system. The chip lets you define as many as 12 independent timing signals by using programmable, registered output waveforms. A resident 10- to 100-MHz multiplying PLL crystal oscillator ensures timing accuracy; however, you must use an external system clock to clock the IC. The Am2971 comes in a 24-pin ceramic DIP and costs $17.75 (100).—J D Mosley

JITTER ATTENUATOR REMOVES 14 UNIT-INTERVALS FROM T1 DATA

Using a PLL and a 16-bit FIFO elastic store, the CSC61600 from Crystal Semiconductor (Austin, TX, (512) 445-7222) filters jitter occuring at frequencies of 250 Hz and higher in T1 phone circuits. Suitable for use in local-area-network gateways and multiplexers, this jitter attenuator also meets the phone company's tolerance and transfer-function requirements. This CMOS chip requires an external 6.175-MHz crystal for clocking to control the FIFO buffer. The device uses one 5V power supply and dissipates 25 mW max of power at 25°C. It costs $4.00 (1000).—J D Mosley

ELECTRICALLY ERASABLE CMOS LOGIC IC SPECS 66-MHz CLOCK RATE

Lattice Semiconductor (Portland, OR, (503) 629-2131) has introduced the industry's first electrically erasable programmable logic device that meets MIL-STD-883C specifications. Fabricated with the company's UltraMOS CMOS process, the GAL16V8-15 draws only 90 mA from a 5V supply over −55 to +125°C and still sustains a maximum clock rate of 66 MHz. It consists of eight 24-mA output logic macrocells, which emulate Monolithic Memories Inc's 20-pin B-PAL devices. Full-production quantities of the 20-pin cerdip device will be available in December; you can get sample quantities now for $25.55 (100).—Denny Cormier

THE GRAPHICS CHIP FOR COLOR-CONSCIOUS ENGINEERS.

Electronic design geniuses have always been colorful but their creations have not. Until recently, data came in grey, black and green.

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CIRCLE NO 16

NEWS BREAKS: INTERNATIONAL

EDITED BY JOAN MORROW

80C86-BASED LAPTOP COMPUTER FEATURES TWO DRIVES

The T1100 Plus, a 10-lb laptop computer, comes with two 3½-in., 720k-byte diskette drives, 256k or 640k bytes of memory, parallel and serial ports, optional 300- and 1200-baud modems, and a keyboard. The system, from Toshiba's Information Systems Div, incorporates an 80C86 processor running at 7.16 MHz — almost twice as fast as IBM's PC Convertible. The 256k-byte model costs $1999, and the 640k-byte version is priced at $2399. They come with a 640×200-pixel, 80-character×25-line LCD.

MATSUSHITA DEVELOPS GaAs OPERATIONAL-AMPLIFIER IC

Matsushita Electron Industry has developed an operational-amplifier IC made of gallium arsenide. Compared with silicon devices, which are limited to a 1-MHz unity gain range, the GaAs IC raises the gain level to 200 MHz, allowing just one chip to be used to amplify image signals. Matsushita's device integrates 18 FETs and 34 diodes on a 0.93×1.18-mm chip. The company expects samples to be available this year.

PRODUCTION STARTS FOR FEEDBACK LASER DIODES

Hitachi Ltd will start commercially producing distributed-feedback-type laser diodes this summer. These devices can transmit data three to six times farther than conventional laser diodes. The HL-1541A transmits data over a fiber-optic cable for a distance of 100 to 200 km at a speed of 1G bps. The HL-1341A features a repeaterless transmission distance of 80 to 100 km at 1G bps. Samples are available for ¥400,000 ($2353) for the 1300-nm-wavelength device (the HL-1341A) and $2941 for the 1550-nm-wavelength device (the HL-1541A).

LIQUID-CRYSTAL TV MEASURES 12.5×6.75 cm

A 12.5×6.75-cm liquid-crystal pocket television receiver from Casio Inc is reportedly the thinnest device of its kind. The 1.35-cm-thin device fits inside a short pocket. Priced at ¥22,000 ($134), the monochrome TV operates for four hours on three batteries.

MITSUBISHI TO STUDY US MARKET FOR ITS AI WORKSTATION

Mitsubishi Electric Corp, which in May announced an artifical-intelligence workstation developed for the Fifth Generation Computer Project, has begun a survey to see if the sequential inference machine should be marketed in the United States. The company initiated the study after receiving a flood of responses from the US after the announcement of its Melcom PSI—a 32-bit artifical-intelligence workstation that incorporates ESP (extended self-contained Prolog); it sells in Japan for approximately ¥20 million ($117,647).

MOST JAPANESE SOFTWARE IMPORTS COME FROM THE US

Approximately 87% of all imported computer programs used in Japan are made in the United States, according to a survey report released by the Software Distribution Promotion Center. Britain was the second-largest supplier, followed by Canada, Austrialia, West Germany, France, and Israel. The most popular type of imported programs are software-development and management-support programs, followed by scientific-computing, word-processing, and database programs.

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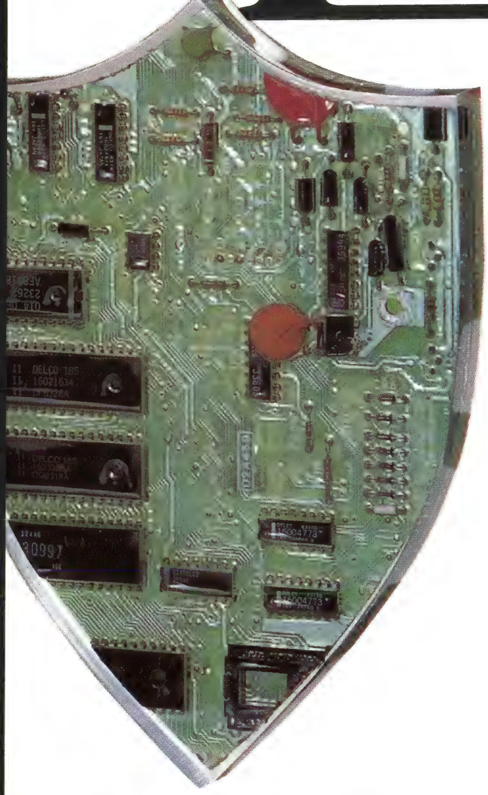

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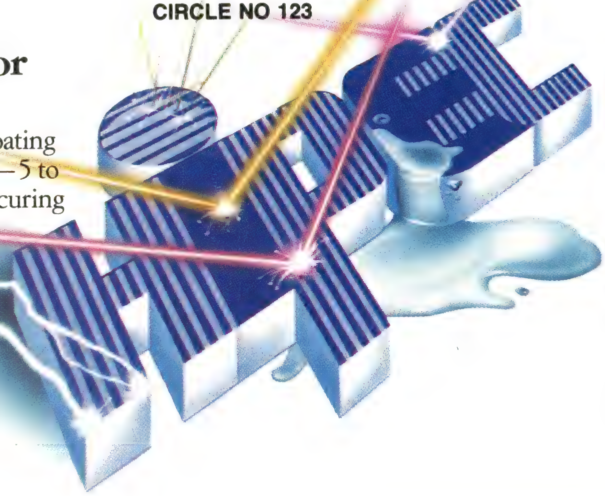
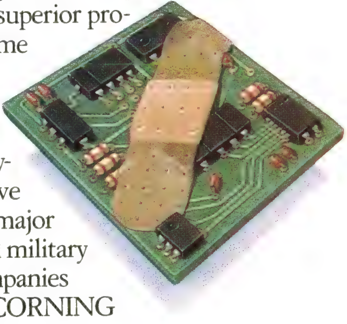


Coating makes repairs on PC boards easier.



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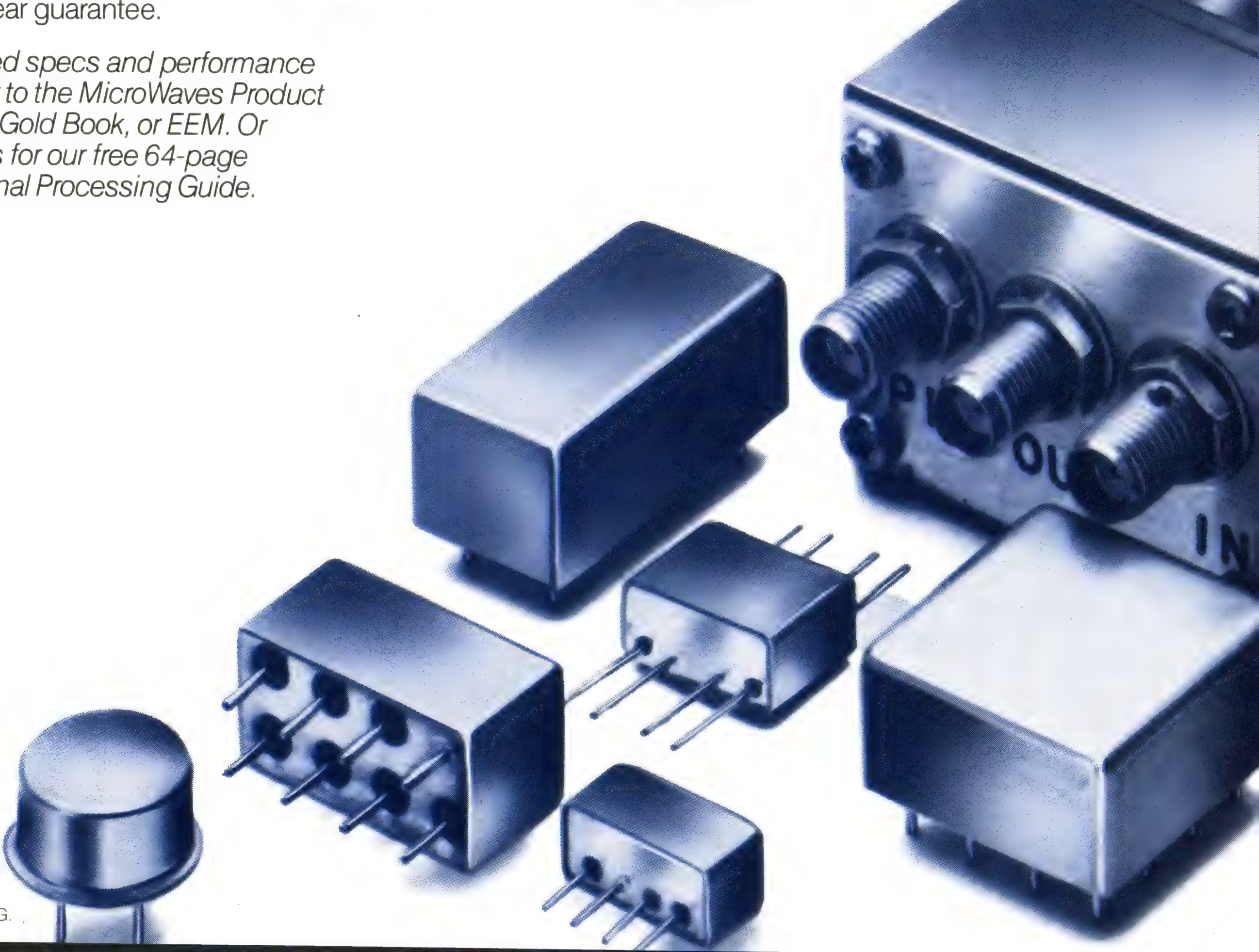
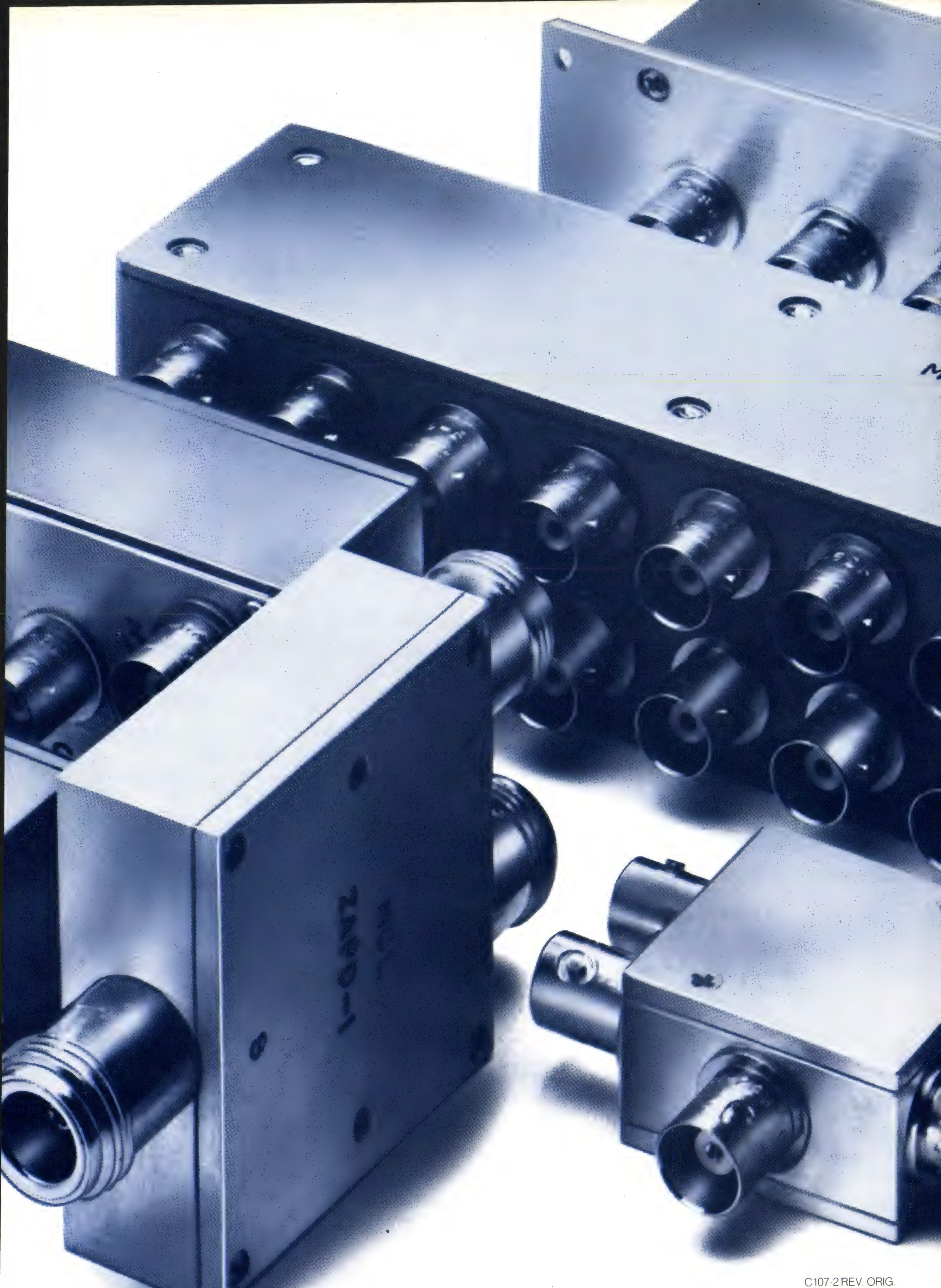


C107-1 REV. ORIG.



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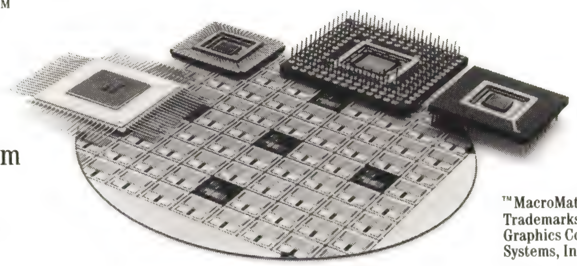

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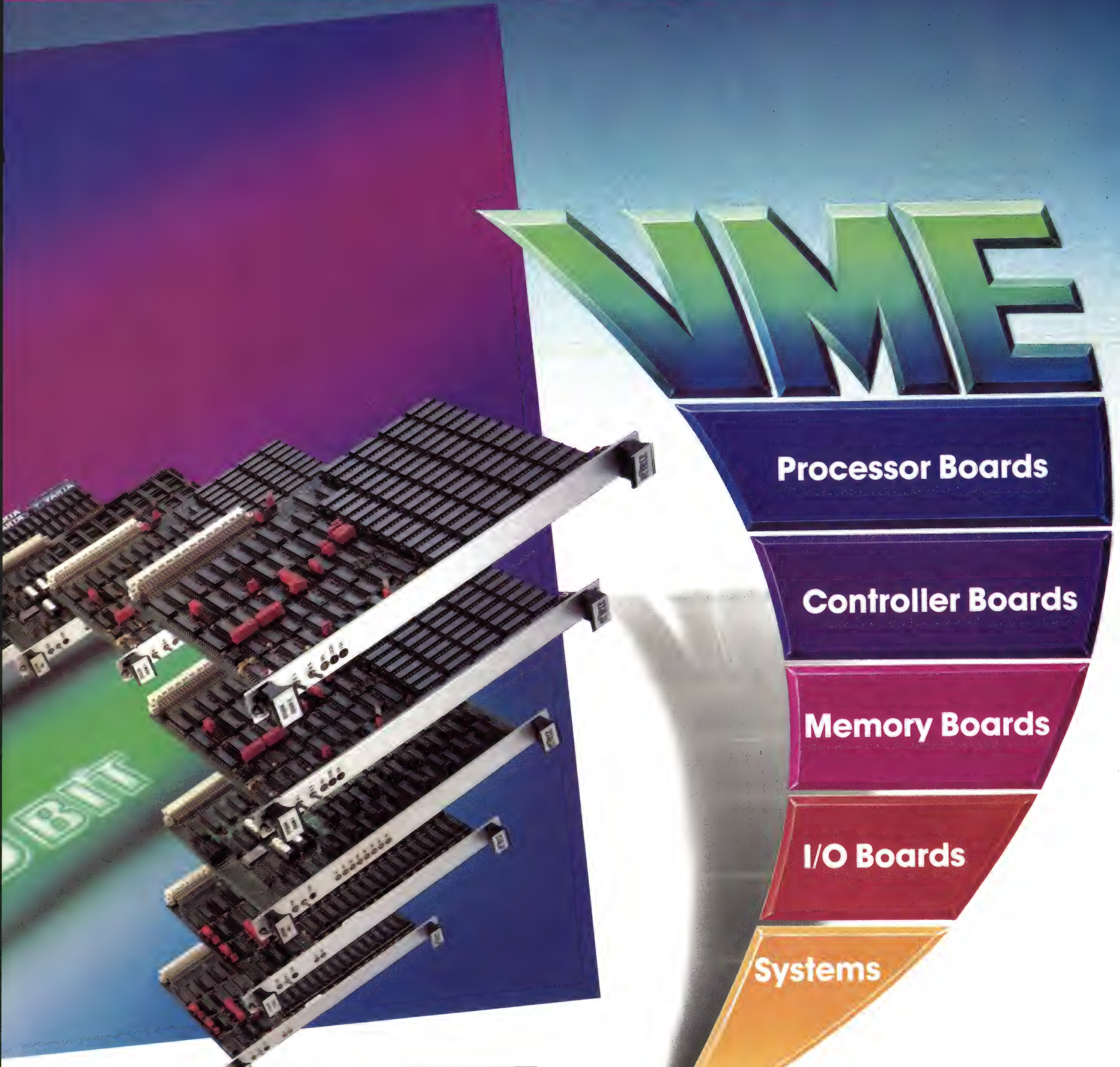

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Model	Capacity	Write/Read (nsec)	Features
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DRAM-2	2MB	190/300	Parity
SRAM-1	128KB	160/160	Bat. Backup
SRAM-2	512KB	160/160	Bat. Backup
RR-1	128KB to 1MB	300/300	RAM/ROM

32 Bit			
Model	Capacity	Write/Read (nsec)	Features
DRAM-E3M/S	1 to 7MB	70/250	Parity
DRAM-E4M/S	4 to 28MB	70/250	Parity
DRAM-5	2 or 4MB	140/270	EDC
SRAM-3	1MB	80/220	Bat. Backup
RR-2	256KB to 2MB	80/220	RAM/ROM

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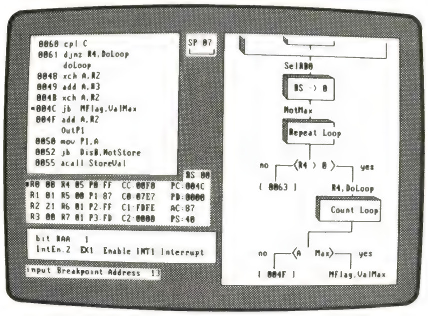

```
 0060 cpl C
 0061 djnz R4,DoLoop
      doLoop
 0048 xch A,R2
 0049 add A,R3
 004B xch A,R2
=004C jb  MFlag,ValMax
 004F add A,R2
      OutP1
 0050 mov P1,A
 0052 jb  DisB,NotStore
 0055 acall StoreVal
```

```
                                           BS 00
*R0 00 R4 05 P0 FF  CC 00F0   PC:004C
 R1 01 R5 00 P1 87  C0 07E7   PD:0000
 R2 21 R6 01 P2 FF  C1 FDFE   AC:87
 R3 00 R7 01 P3 FD  C2 0000   PS:40
```

```
bit NAA   1
IntEn.2  EX1  Enable INT1 Interrupt
```

```
input Breakpoint Address  13
```

(8051 debug/simulator shown)

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SIGNALS & NOISE

Perceived risk determines salaries

Dear Editor:

I have just read your editorial "Engineers, managers, and the money stream," which appeared in the June 12 issue of EDN (pg 51). Although I agree with the apparent results, because the statistics prove it, my experience tells me that the cause your editorial suggests is not a cause but a result.

The cause is risk. There is greater risk in being a salesman than in being a design engineer. There is greater risk in being a sales manager than in being an engineering manager.

Perceived risk is the main salary driver. The proximity to the money stream is a function of risk. Too many people, blue-collar workers and engineers alike, want the reward but are unwilling to take the risk.

The way to get more money is to elevate the perceived degree of risk that a position requires. Examples of this fact abound. Garbage collectors often command higher salaries than firemen do. The reason is that the public perceives the risk of having garbage pile up in the streets to be greater than that of having a fire. Japanese workers have lower salaries than their American counterparts, in part, because their job risk is lower. Even in this country, many workers have been willing to accept lower pay if their job risk is lower.

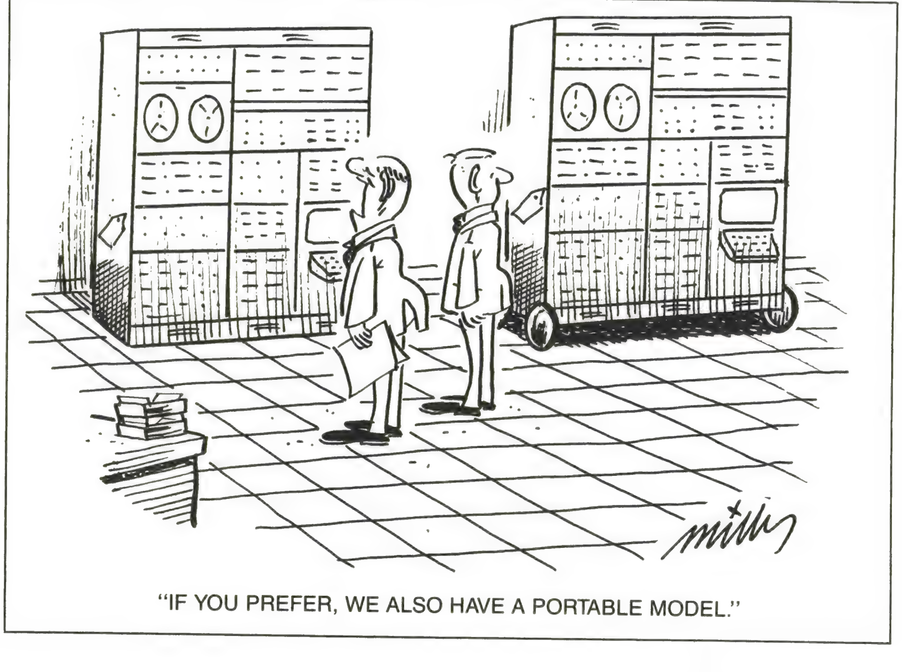
I get somewhat annoyed when people, engineers or otherwise, having complained about their lower salaries, refuse a position with a higher salary but with a higher perception of risk.

Sincerely yours,
J D Baugher
Engineering Manager
Sorensen Co
Manchester, NH

Minorities don't deserve special treatment

Dear Editor:

Let me compliment you on a generally excellent publication. However, I find it very disturbing that magazine space has been given over to the typical feminist/liberal whining that distorts national statistics concerning minorities. I refer to the heavily biased article "Efforts to draw minorities to engineering make progress but still face obsta-



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CIRCLE NO 19

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SPRAGUE
THE MARK OF RELIABILITY

CIRCLE NO 21

cles" by Deborah Asbrand (EDN, May 29, pg 259).

What engineering (and this country) does not need is the neo-socialistic numbers game, a quota system, or special privilege for a few, which feminists in particular are trying to impose on this society. The government, at any level, has no constitutional mandate to encourage anyone to, or discourage anyone from, anything. If government has a role, it's to reinstate meaningful education in the public school system and to eliminate the left-wing political activity—as well as all political activity—of the teachers' unions.

What is desperately needed is the return to a strong commitment to higher academic standards and individual responsibility, and a strong denunciation of this endless agitation from the left for preferential treatment of certain groups.

Sincerely yours,
Thomas Silhan
Baltimore, MD

Company's 8-bit ADCs are sampling converters

Dear Editor:

I would like to commend Tarlton Fleming on his recent Special Report on data converters (EDN, May 29, pg 102). I must, however, correct a slight error. The article reported that three of Analog Devices' 8-bit A/D converters were "not sampling converters."

On the contrary, the 1.36-μsec AD7820, the 2.5-μsec, 4-channel AD724, and the 2.5-μsec, 8-channel AD7828 all use a half-flash conversion process that incorporates sampled data comparators. These comparators are ac coupled, via on-chip capacitors, to remove their dc offset voltage. It is a simple matter to make these coupling capacitors store the input voltage, thus providing a track/hold or sample/hold function.

The built-in track/hold function for the 7824 and 7828 is guaranteed to capture signals with slew rates as high as 157 mV/μsec, which corresponds to a full-scale sine-wave signal of 10 kHz. The 7820 guarantees 100 mV/μsec, which corresponds to 7 kHz.

Sincerely yours,
Mark Logan
Technical Publicity
Analog Devices
Norwood, MA

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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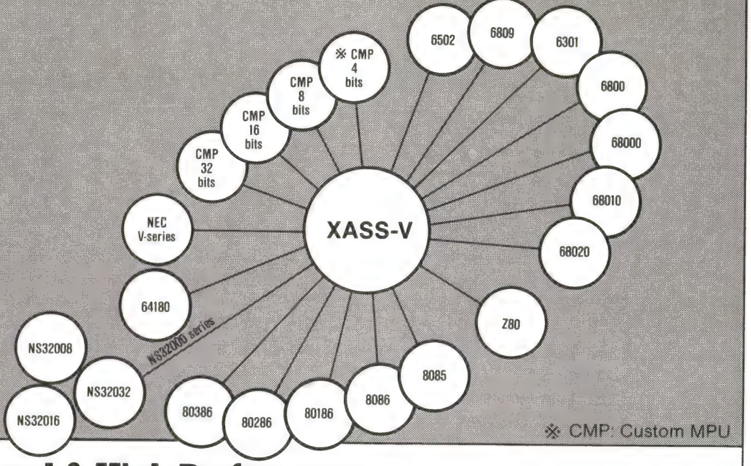

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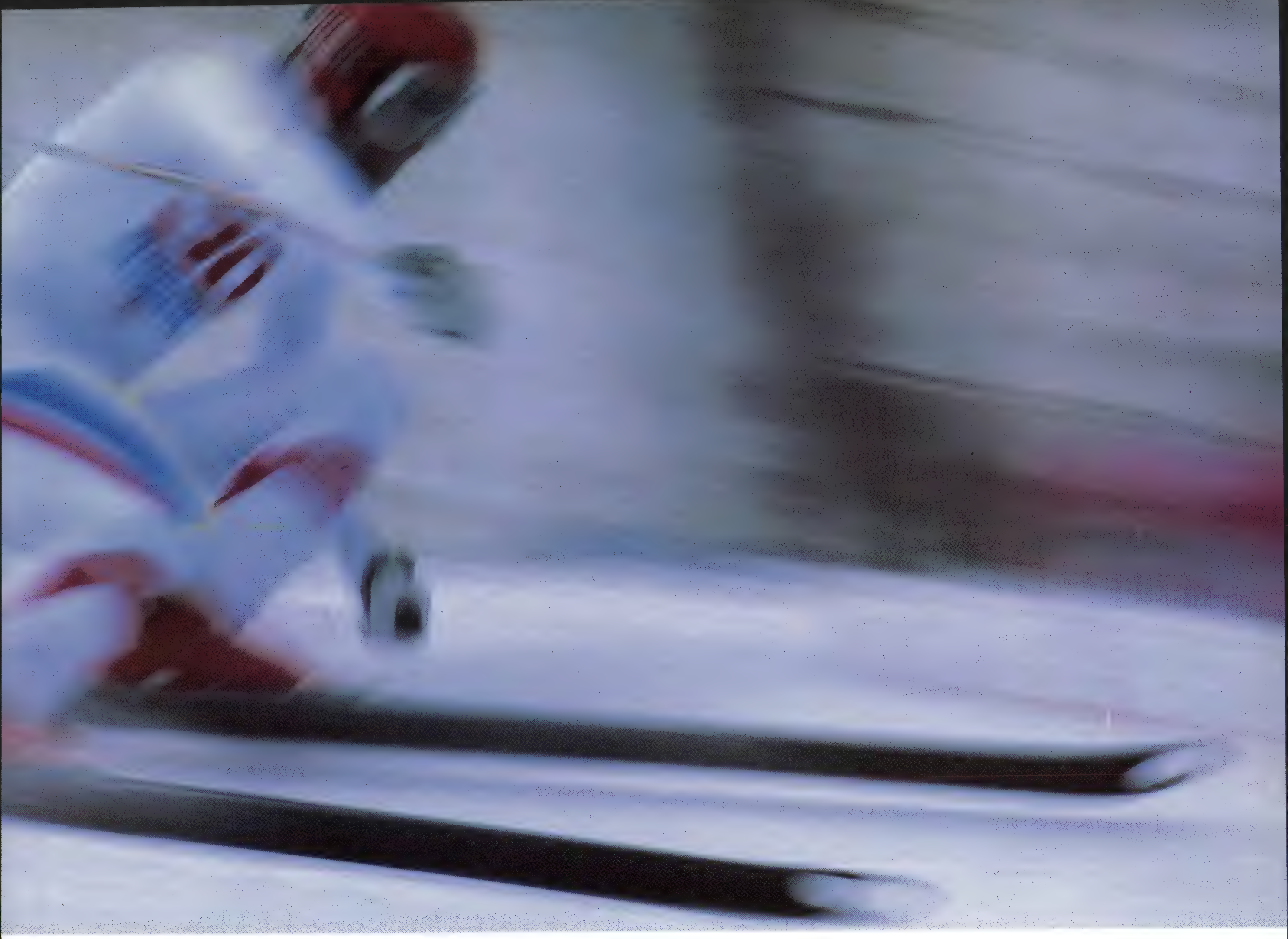

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IMS2800-80		43ns	80ns	146ns
IMS2800-10		53ns	100ns	176ns

Part Number	Function	Column Access Time (Max.)	$\overline{\text{CAS}}$ Access Time (Max.)	Page Mode Cycle Time (Min.)
IMS2801-60*	Enhanced Page Mode	32ns	11ns	35ns
IMS2801-80		43ns	13ns	46ns
IMS2801-10		53ns	16ns	56ns

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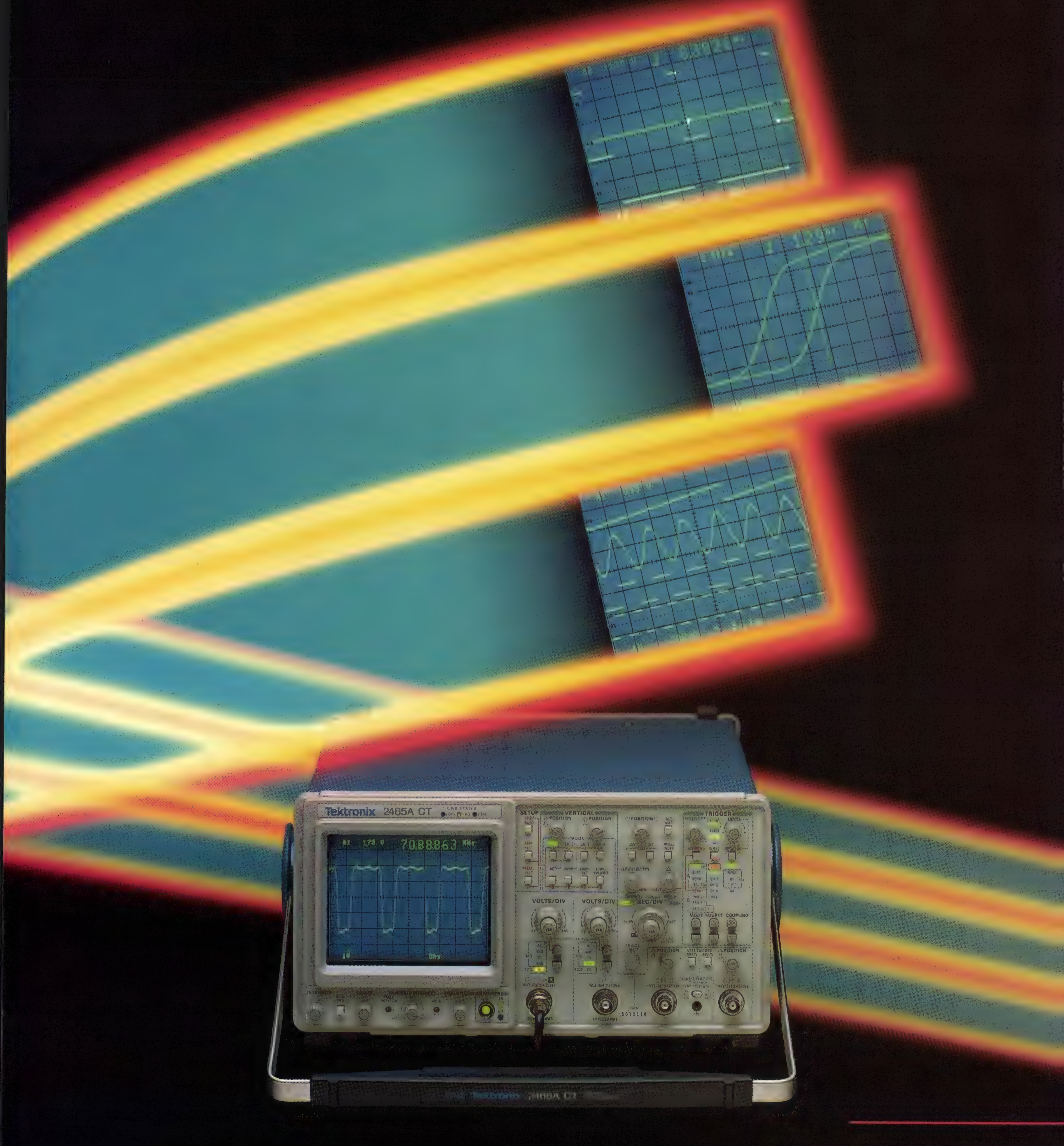

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The Tektronix 2445A/2465A Family brings new convenience to leading-edge performance. Start with standards set by Tek's top portable analog scopes. Add new productivity-enhancing features for fast operation. And increase the 2465A bandwidth to 350 MHz.

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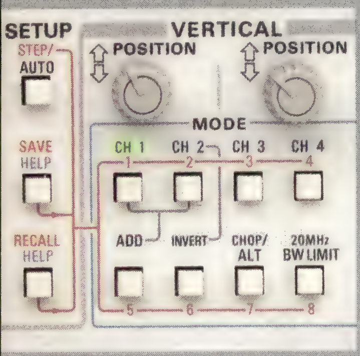

New AUTO-SETUP, SAVE/ RECALL and SETUP SEQUENCING give the 2445A/2465A Family stand-alone automation—and enhance *your* productivity.

See your signals on screen in less time, automatically. Attach up to four probes to signal points, press AUTO-SETUP, and within seconds a stable, automatically triggered display of your probed waveform appears on screen for quick viewing or advanced parametric characterization.

Measure signal parameters more quickly with instant access to complex setups. The new SAVE/ RECALL utility makes switching between measurements fast—just two buttons for a complete setup. And operator attention is focused on answers, not on control adjustments.

Non-volatile memory for 30 setups stores all front-panel information, including cursor locations and control settings for the extended measurement options. You can also store seven-character alphanumeric labels with each setup—as test titles or even operator prompts. HELP message makes operation even easier.

Automate repetitive measurement sequences without an external controller—and without writing a single line of code. Now set up, store and sequence systematic verification procedures for engineering prototypes, production test or field service without a computer. Using the STEP button or an external switch you can step through up to 30 setups in the order you choose.

Features	2465A	2445A
Probe Tip Bandwidth	350 MHz	150 MHz
No. of Input Channels	4	4
Channel 1/Channel 2 Vertical Sensitivity	2 mV/div to 5 V/div	2 mV/div to 5 V/div
Channel 1/Channel 2 Accuracy	2%	2%
Channel 1/Channel 2 Input Couplings	1MΩ: DC, AC and GND 50Ω: DC	
Max. Sweep Speed	500 psec	1 nsec
Max. Timing Accuracy	.55%	.55%
Trigger Frequency	500 MHz	250 MHz
Trigger Modes	Auto Level, Auto, Norm and Single Sequence	
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A wide range of vertical sensitivities and sweep speeds plus powerful triggering capabilities make it easy to study a tremendous variety of analog and digital signals. All with push-button convenience.

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CIRCLE NO 24

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CMOS silicon-on-sapphire (SOS), with its unique ability to withstand transient bursts of energy, is ideal for radiation hardened military ground systems.

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RCA provides gate arrays or standard cell application specific ICs in standard CMOS as well as CMOS/SOS for special Rad-Hard applications. Our designer-friendly software and worldwide design center locations make semicustom simple.

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CIRCLE NO 26

CALENDAR

World Computer Congress, International Federation for Information Processing (IFIP '86), Dublin, Ireland. David Hyatt, Data Decisions, 20 Brace Rd, Cherry Hill, NJ 08034. (609) 429-7100. September 1 to 5.

Comdex/Australia, Sydney, Australia. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. September 2 to 5.

IEEE Eascon '86 (IEEE Electronics and Aerospace Systems Conference), Washington, DC. Eascon '86, Suite 300, 655 15th St NW, Washington, DC 20005. (202) 639-4374. September 8 to 10.

NCC-Telecommunications Conference, Philadelphia, PA. AFIPS, 1899 Preston White Dr, Reston, VA 22091. (703) 620-8900. September 8 to 10.

Midcon, Dallas, TX. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. September 9 to 11.

Modern Electronic Packaging, Santa Clara, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 9 to 11.

International Videotex Industry Exposition and Conference, New York, NY. Videotex Industry Association, 1901 N Fort Myer Dr, Suite 200, Rosslyn, VA 22209. (703) 522-0883. September 15 to 17.

Printed Wiring Board Assemblies —Processes, Techniques, and Equipment (short course), Milwaukee, WI. Peter Tocups, Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. September 15 to 17.

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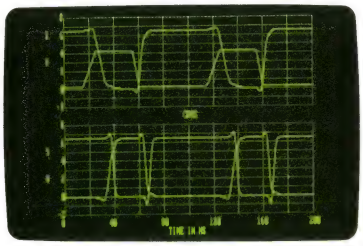
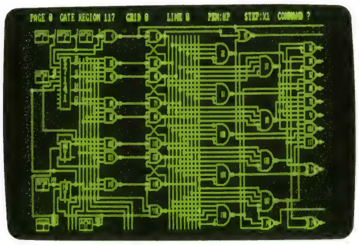

"Typical MICROCAP Transient Analysis"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Regarding MICROCAP . . . "A highly recommended analog design program" (PC Tech Journal 3/84). "A valuable tool for circuit designers" (Personal Software Magazine 11/83).

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CIRCLE NO 27

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CIRCLE NO 28

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CALENDAR

Euromicro '86 (Symposium on Microprocessing and Microprogramming), Venice, Italy. Euromicro Box 217, 7500 AE Enschede, Th Netherlands. (31) (53) 338799. September 15 to 18.

Modern Power Conversion Desig Techniques (short course), Sant Clara, CA. E/J Bloom Associates 115 Duran Dr, San Rafael, C 94903. (415) 492-8443. September 1 to 19.

5th Annual Conference of th American Voice I/O Society, Alexandria, VA. American Voice I/O Society, Box 60940, Palo Alto, C 94306. (408) 742-2539. September 1 to 18.

Fall National Design Engineerin Show and Conference, New York NY. Cahners Exposition Group, 99 Summer St, Stamford, CT 06905 (203) 964-0000. September 16 to 18

Semicon/East '86, Boston, MA Semiconductor Equipment and Materials Institute, 625 Ellis St, Suite 212, Mountain View, CA 94043 (415) 964-5111. September 16 to 18

Sensors Expo, Chicago, IL. Expocon Management Associates, 369 Post Rd, Southport, CT 06490. (203 259-5734. September 17 to 19.

IBM PC Microcomputer Interfacing, Scientific Instrument Automation, and Control, Charlotte NC. Center for Continuing Education, Virginia Tech, Blacksburg, VA 24061. (703) 961-5182. September 18 to 20.

12th European Conference on Optical Communication, Barcelona, Spain. Central de Congresos, SA, Avda General Peron, 26, 28020 Madrid, Spain. (34) (1) 4551088. September 22 to 25.

Ultratech '86, Long Beach, CA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-0023. September 22 to 25.

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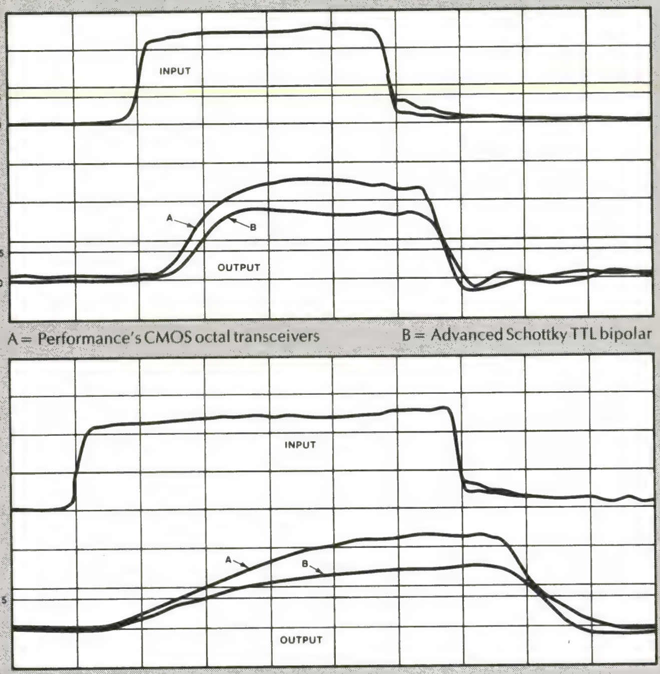

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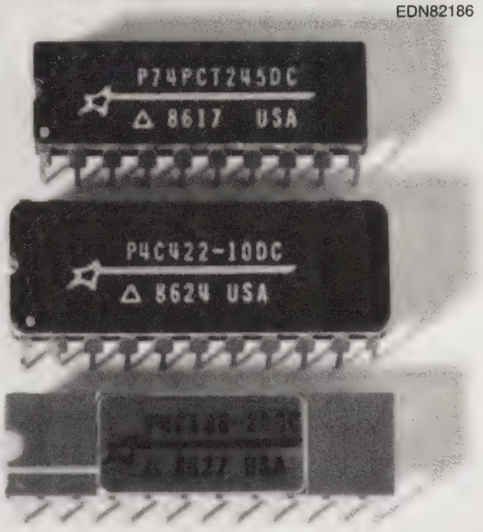

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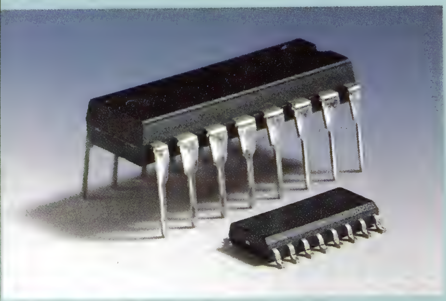
Available through our extensive European organisation, Philips HCMOS is on-hand wherever you are. Don't look overseas for your HCMOS needs; save time and come to us, the largest European source.



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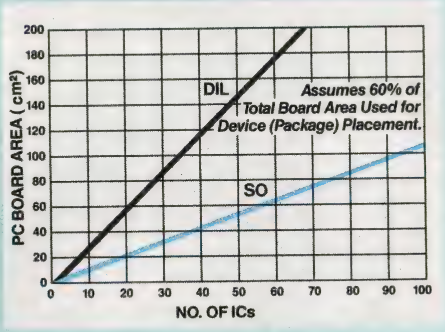

Save board space. Our SO-versions are up to 65% smaller than comparable DILs, and are up to 10 times lighter.

Need samples or data? Then call your local Philips organisation (see below). We're ready with full technical support and documentation. Plus a Designer's Guide, set to become the standard for designing with HCMOS.

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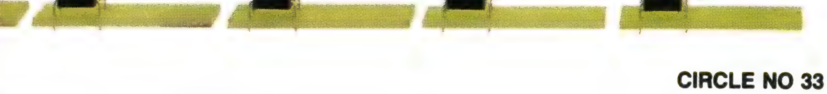

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EDITORIAL

Evolving computer technology and engineering opportunities

Computers are undoubtedly important tools in your work. However, you probably find that the direct influence you exert on the selection and purchase of personal computers, engineering workstations, and associated software abates when more expensive products are considered. For example, if you make use of a mainframe on a timesharing basis, you probably feel somewhat removed from the specifying decision, especially if you work for a large company. In such cases, the purchasing decision was probably made by a group close to the money stream (see "Engineers, managers, and the money stream," EDN, June 12, 1986, pg 51), and not by an engineer.

The result of this situation is that you're likely to find little opportunity to become familiar with the capabilities of high-performance, high-priced computer equipment. This isolation will become increasingly unfortunate with the advent of parallel processors and supercomputers. These computers can serve in a variety of engineering applications, but the current trend is for them to operate transparently as far as the engineer is concerned. For example, Fairchild uses a Cray 1S for gate-array design, but VAX minicomputers serve as front ends that isolate users from the Cray, as Staff Editor George Stubbs notes in "Industry needs design-automation experts to unleash the power of supercomputers" (EDN, August 7, pg 259). Such isolation is worsened by the emergence of AI programs that, although they simplify user/machine interaction, hide the details of computer operation from the user (see "Will AI do it all for you?" EDN *Career News*, June 1986, pg 1).

The intention, understandably, is to minimize the retraining required to make use of more powerful computers and software. However, the drawback of this isolation is that it exacerbates the shortage of engineers qualified to exploit the full power of high-performance computers—those who understand the details of the application and the techniques of vector processing and expert-system development.

But this shortage in turn opens up opportunities for the aggressive engineers with applications expertise—engineers who are willing to acquire supercomputer or AI expertise. Although many top specialists in these fields will come from universities, an expert from industry is well placed to make a significant contribution. Indeed, cooperation between industry and academia is becoming invaluable. The June issue of EDN *Career News*, for example, profiles a software development manager from Digital Equipment Corp who worked with a team of AI experts from Carnegie-Mellon, MIT, and Stanford to develop the Common Lisp dialect. Such cooperation should be similarly helpful in the development of, for instance, CAE simulation programs that run on Cray-level machines.

For its part, EDN will keep you informed with overviews—such as the one on parallel processors on pg 75 and the one on artificial intelligence scheduled for later this year—of these important topics. Although you might not have immediate application for such computers and software, these articles can serve as a starting point as you acquire the expertise that will help you make use of—and contribute to the development of—these computers and software as the technology evolves.

Rick Nelson

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Managing Editor

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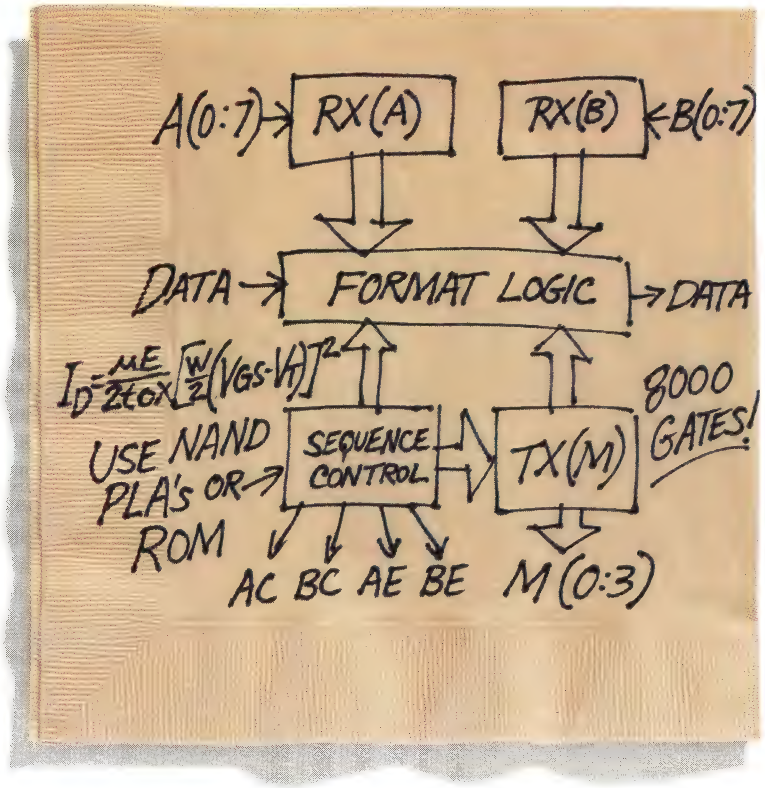

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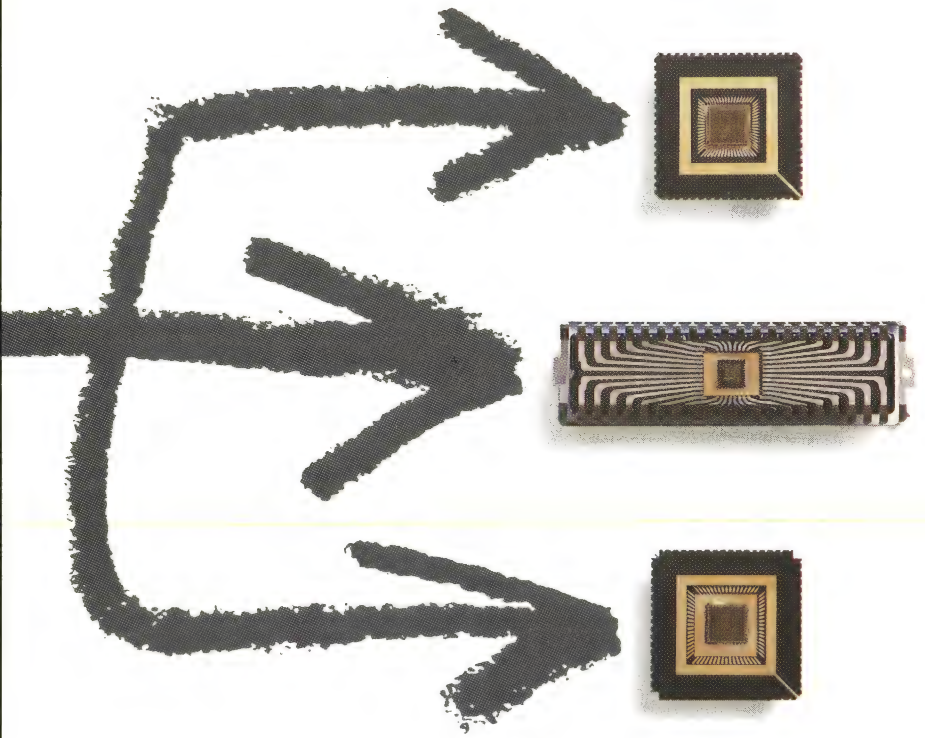

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TECHNOLOGY UPDATE

Phase-locked loops and frequency dividers handle higher-speed circuit functions

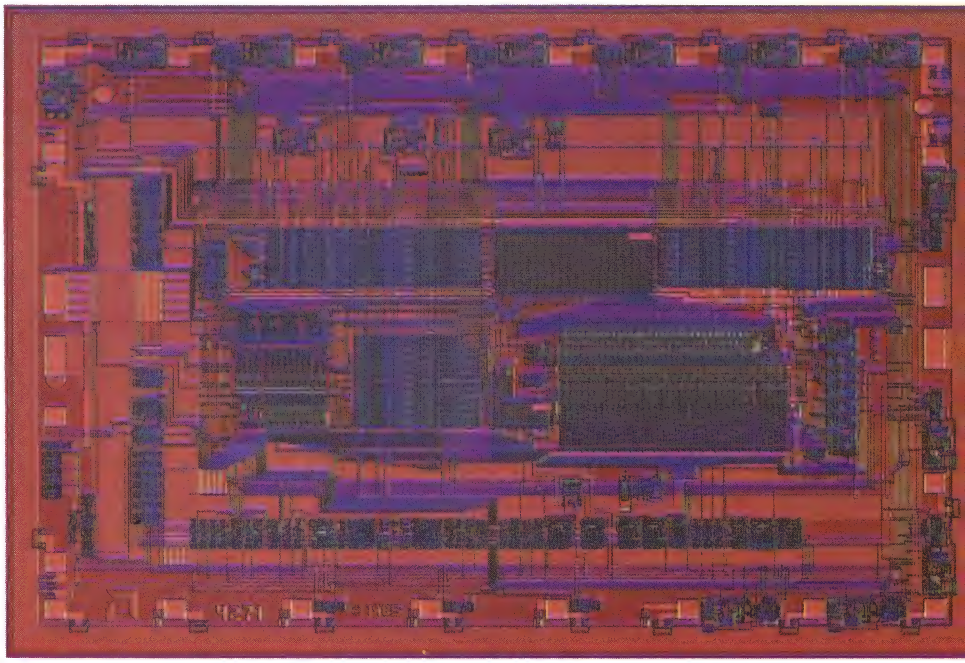
Bill Travis, *Senior Editor*

Several recently introduced frequency-manipulating ICs use phase-locked loops (PLLs) and digital counter (divider) circuitry to achieve a variety of results—for example, FM demodulation, frequency division and multiplication, and timing-resolution enhancement. The new ICs handle higher frequencies than their predecessors, and some now employ gallium arsenide (GaAs) technology. What's more, families of custom and semicustom GaAs ICs may serve your needs if you have special frequency-division requirements.

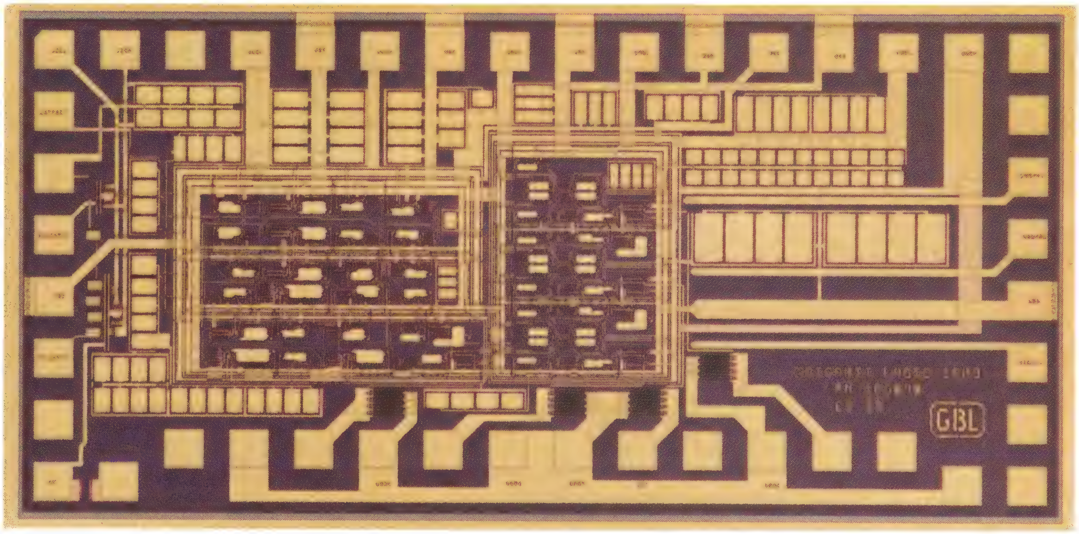
PLLs and frequency dividers differ fundamentally. In PLLs, an internal oscillator locks its frequency to the IC's input frequency or to a multiple or submultiple thereof. A phase detector provides the locking action by feeding back a voltage or current output that's proportional to the difference in phase between the input signal and the oscillator output. In addition to the locking action, the fed-back phase-difference signal can accomplish other useful functions—for example, FM demodulation.

On the other hand, a dedicated frequency-divider circuit, or prescaler, uses combinatorial- and sequential-logic blocks to effect some predetermined exact division of the input frequency. Such ICs, therefore, are strictly digital circuits; a PLL device usually combines digital and analog circuitry.

If a hall of fame existed for PLL ICs, Signetics's venerable SE/NE564 and SE/NE565 PLLs would be prime candidates for nomination to the institution. (The SE and NE prefixes designate the −55 to



Using a PLL to multiply the clock frequency, *the Am2971 programmable event generator (top) from Advanced Micro Devices offers a timing resolution of 10 nsec.*



This 2-GHz variable-modulus divider on a GaAs chip, *the 10G070 from GigaBit Logic (left), is useful in UHF synthesizer applications.*

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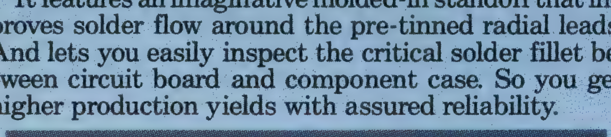

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+125°C and 0 to 70°C operating-temperature ranges, respectively.) Introduced back in the days when dynamic RAMs were a profitable commodity, these devices have earned firm industry-standard status.

Models SE/NE564 and SE/NE565 are 50-MHz and 500-kHz PLLs, respectively. A new device, currently available in sample quantities, extends the frequency limit to 150 MHz. Model SE/NE568 comprises a preamplifier, a level-shifting circuit, current-to-voltage and voltage-to-current converters, an output buffer, a current-controlled oscillator, and bias circuitry that incorporates temperature- and frequency-compensation characteristics.

Appropriate for such applications as satellite receivers, fiber-optic video links, and VHF frequency-shift-keyed (FSK) demodulators, the SE/NE568 is particularly well suited to the task of demodulating wide-deviation FM signals in systems requiring a very linear output. In the 70-MHz satellite-receiver application shown in **Fig 1,** for example, the device exhibits less than 4% nonlinearity (1.5% typ) when demodulating ±10% frequency deviations.

Note that the SE/NE568 offers loop-filter terminals; you can connect external capacitors and resistors to these terminals to configure first- or second-order filters. Packaging options include a 20-pin DIP and a 20-lead SO (small-outline), surface-mountable plastic package. Although samples are available now, production prices are yet to be determined.

Multiplying PLL hikes resolution

A PLL oscillator's ability to lock the generated frequency to an external frequency source can be a valuable attribute. The value increases further when you consider that the oscillator's frequency need not be restricted to that of the input, but can instead be a multiple or submultiple of the input frequency. By exploiting this frequency-multiplying ability, the Model Am2971 programmable event generator **(Fig 2a)** from Advanced

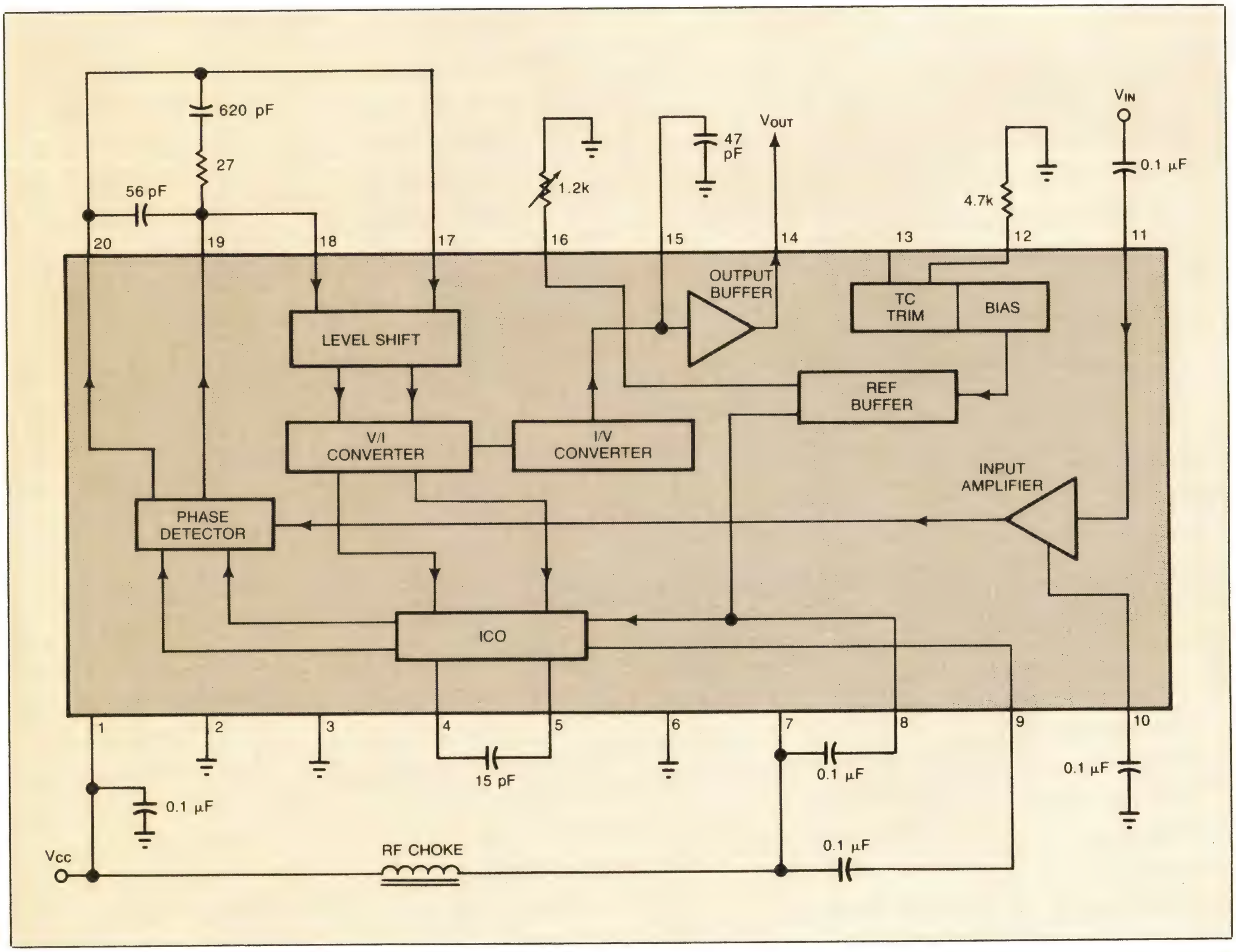

Fig 1—Able to accommodate input frequencies as high as 150 MHz, *the SE/NE568 PLL from Signetics is eminently suitable as an FM demodulator in high-frequency receivers. The IC uses a current-controlled oscillator, in contrast with most PLLs' VCOs. The device provides terminals you can use to insert loop filters.*

Micro Devices offers high-resolution timing control.

Using PROM-type fuse technology, the Am2971 allows you to program as many as 12 registered output waveforms for use in timing applications. Thanks to its embedded, multiplying PLL oscillator (in the clock-control section of the block diagram), the IC can produce programmable event intervals having resolution as fine as 10 nsec.

The Am2971's onboard multiplying PLL oscillator generates frequencies ranging from 70 to 100 MHz; the IC's clock output has a user-selectable frequency of ⅕ or ⅒ the PLL's frequency. **Figs 2b** and **2c** give the clocking options for the device. In **2b,** an external clock synchronizes the PLL's oscillator to a frequency five or 10 times the clock frequency. In **2c,** a 7- to 20-MHz crystal drives the PLL. The manufacturer recommends you use an AT-cut, parallel-resonant crystal.

Eight fuses in the IC allow you to set the internal clock frequency as a function of the crystal's or the input clock's frequency. The choices for the frequency of the internal clock are one, five, 10, 5/2, or 5/4 times the input frequency. Two other possibilities, 10/2 and 10/4, obviously give the same internal-clock-rate results as five and 5/2, respectively.

You choose one of eight start addresses to begin the Am2971's tim-

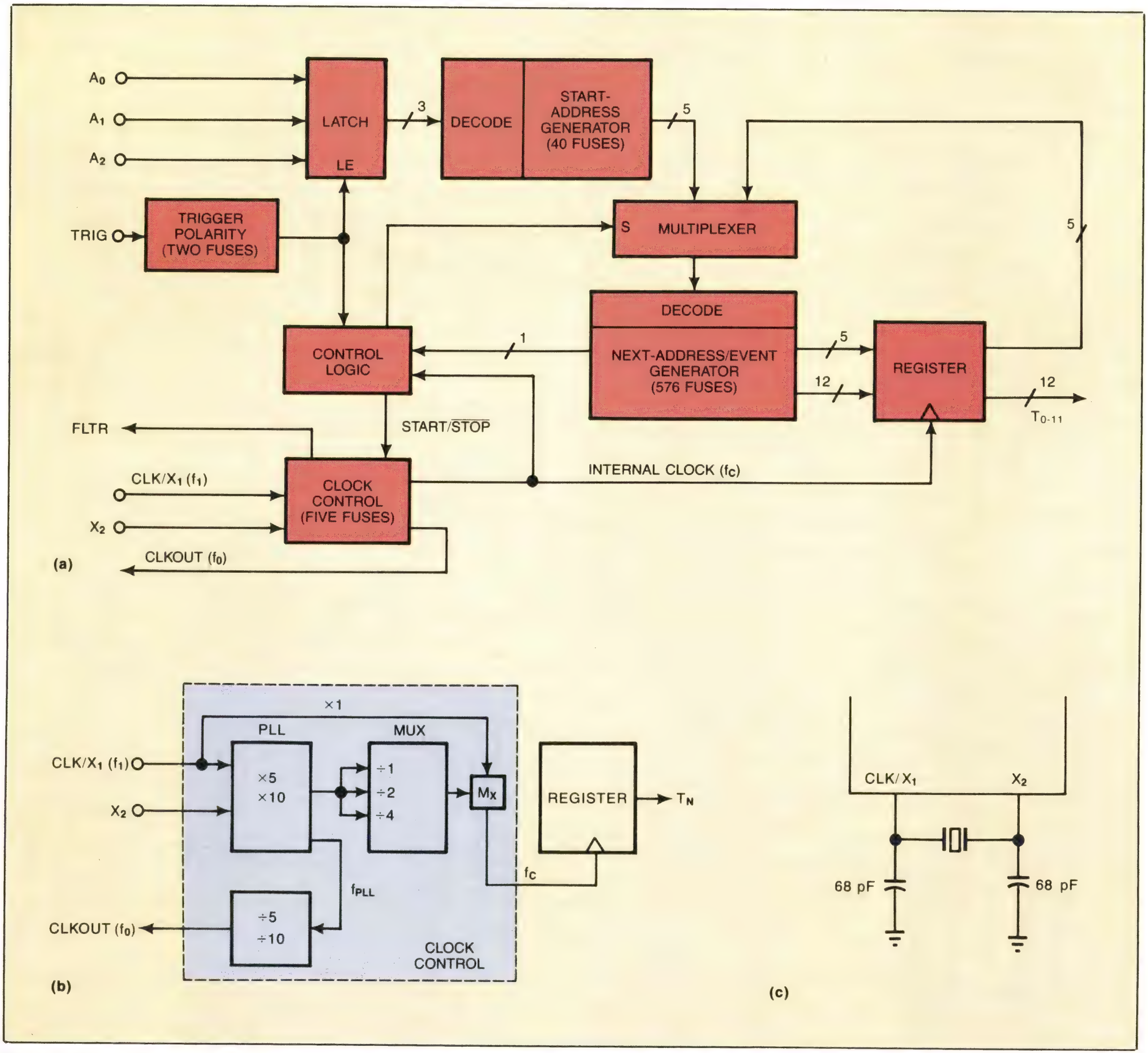

Fig 2—The oscillator in a PLL need not lock to the exact frequency of the input. *In the Am2971 programmable event generator from Advanced Micro Devices, the PLL provides a timing waveform whose frequency is a programmable multiple of the input clock's repetition rate. The net result is an enhancement of the time resolution in setting timing intervals. You can use either an external clock* ***(b)*** *or a crystal* ***(c)*** *to set the reference frequency.*

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ing sequence. The IC's fuses give you programmable control of the timing sequence's start and stop functions. One appropriate application for the device is as a digital substitute for analog delay lines (for example, to generate the complex clock signals needed by address-multiplexed dynamic RAMs).

Other applications for the Am2971 include bus timing or peripheral control—for example, in disk-drive control or as the timing controller for bit-mapped graphics systems. Housed in a 24-pin ceramic DIP, the Am2971 costs $17.75 (100). Future packaging options will include a ceramic LCC and a J-leaded PLCC.

One useful class of ICs performs programmable frequency division and provides a phase-comparator output to an external VCO. These frequency-synthesizer ICs contain all the logic and phase-detection circuitry needed to configure VHF-band PLLs. An example of these synthesizer ICs is Plessey's CMOS-processed NJ88C30 (**Fig 3**).

For its frequency reference, the NJ88C30 uses an external, parallel-resonant crystal whose fundamental frequency can be as high as 15 MHz. The IC's sensitivity to the input signal from the external VCO is a function of frequency; it typically varies from 0.1V rms at 100 MHz to 0.5V rms at 200 MHz. The guaranteed sensitivity for any frequency to 200 MHz is 1V rms. The NJ88C30 costs $4.80 (1000) in a plastic DIP.

As you can see in the block diagram, the synthesizer chip contains a reference oscillator and divider, a dual-modulus (÷15/16) prescaler and associated 4-bit control register, a 12-bit programmable divider, a phase comparator, and all necessary data-input and control logic.

Table 1 shows the comparison frequencies derived from the divider in the frequency-reference chain, for all possible combinations of the first three bits of input data. You select the IC's overall division ratio by loading a 16-bit word through the serial data bus. The ratio can vary from 240 to 65,535; the VCO's frequency in a locked system is this division ratio multiplied by the comparison frequency.

In a VHF broadcast receiver, the NJ88C30 can drive a varicap-con-

TABLE 1 — COMPARISON FREQUENCIES IN NJ88C30 SYNTHESIZER

DATA BITS			DIVISION RATIO	COMPARISON FREQUENCY (10-MHz REF OSCILLATOR)
DR_2	DR_1	DR_0		
0	0	0	1600	6.25 kHz
0	0	1	800	12.5 kHz
0	1	0	400	25 kHz
0	1	1	200	50 kHz
1	0	0	2000	5 kHz
1	0	1	1000	10 kHz
1	1	0	500	20 kHz
1	1	1	100	100 kHz

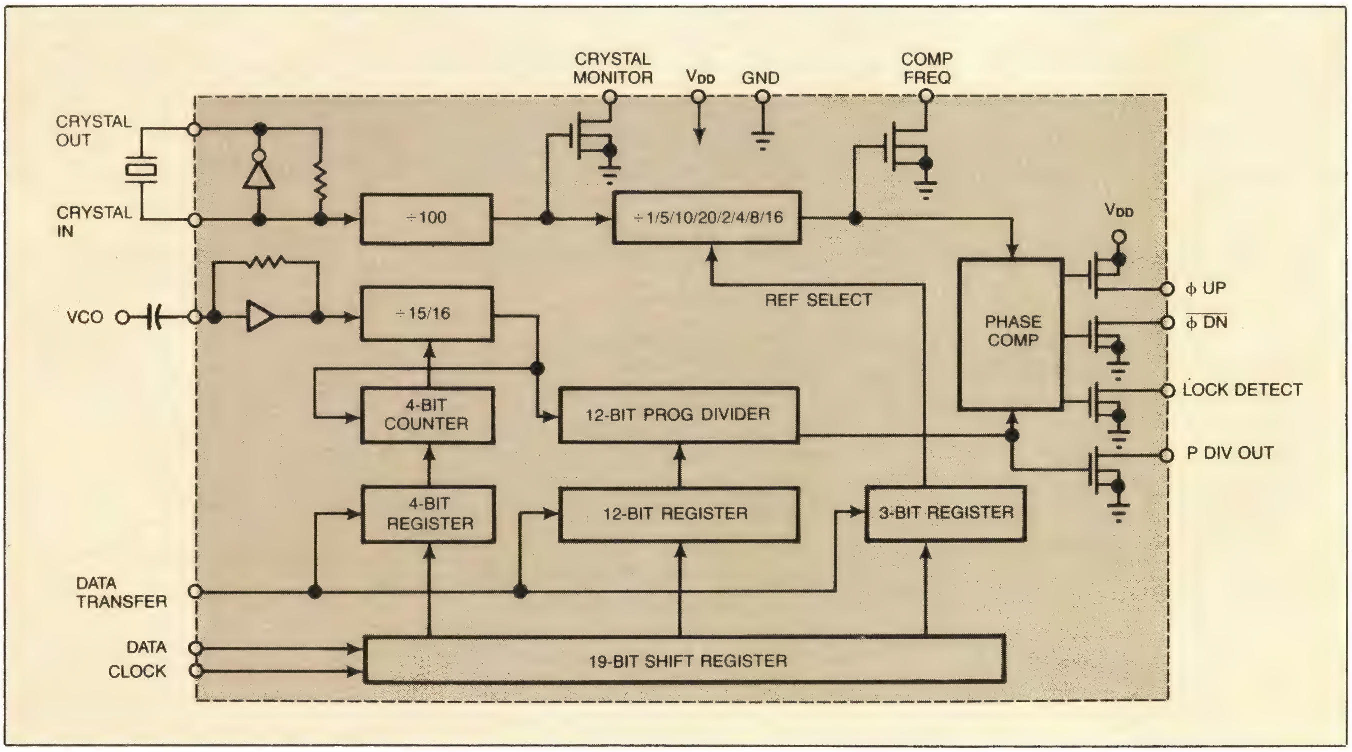

Fig 3—Designed to divide the oscillation frequency of an external VCO, *the NJ88C30 synthesizer from Plessey accommodates VCO frequencies as high as 200 MHz. An external crystal provides the IC's frequency reference. You select the device's overall frequency-division ratio by loading a 16-bit word into the serial data bus.*

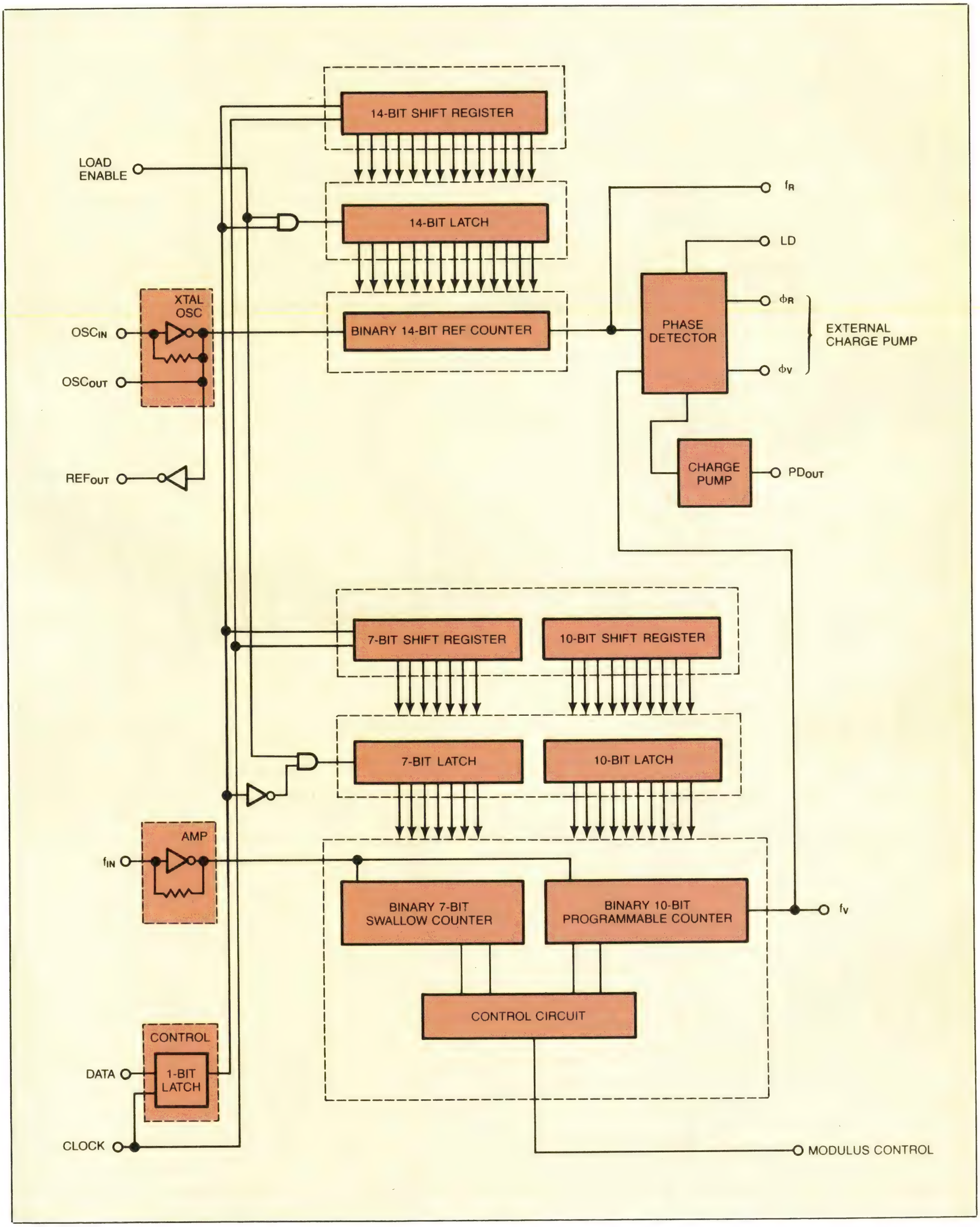

***Fig 4—Serial input data programs the frequency-division ratio** in the MB87006A synthesizer from Fujitsu. You use the IC in tandem with an external dual-modulus prescaler. The synthesizer sets the frequency of an external VCO at an exact multiple of the IC's internally generated reference frequency.*

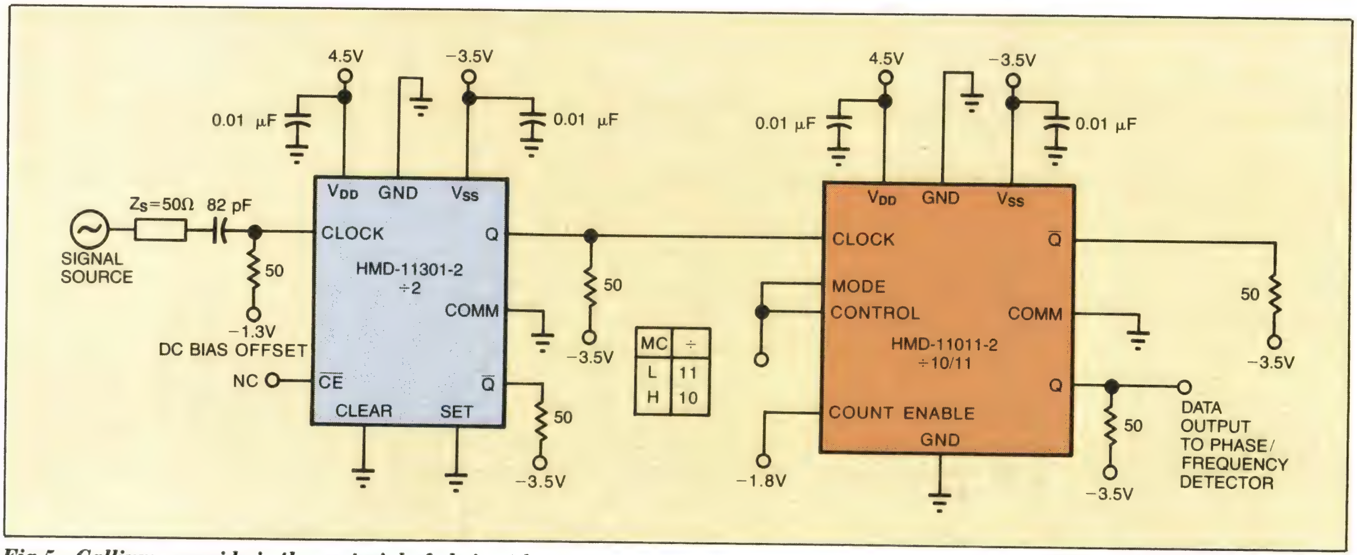

Fig 5—Gallium arsenide is the material of choice *when you need to divide frequencies much in excess of 1 GHz. This divide-by-20 or -22 circuit uses GaAs circuits from Harris Microwave Semiconductor; the circuit accommodates input frequencies as high as 2.5 GHz. A single mode control sets the division ratio to 20 or 22.*

trolled oscillator. The device provides drive voltages as high as 5V; to drive varicaps requiring higher voltages, you can use an op amp at the NJ88C30's output. Note that you should filter the output pulses from the phase comparator; a single-pole RC filter is adequate for the task.

A similar synthesizer from Fujitsu, the MB87006A **(Fig 4),** also uses CMOS circuitry and accepts serial input data for programming frequency-division ratios. The IC is designed to work in conjunction with an external dual-modulus prescaler, such as the company's MB501. The MB87006A costs $4.57 (1000).

The frequency of the VCO connected to the MB87006A is determined by the expression $f_{VCO}=((N\times M)+A)f_R\div R$, where N is the division factor (16 to 1023) of the 10-bit progammable counter; M is the modulus factor (64 in 64/65 mode, 128 in 128/129 mode) of the external dual-modulus prescaler; A is the preset division ratio (0 to 127) of the 7-bit swallow counter; f_R is the output frequency of the reference frequency divider (at the phase-comparator input); and R is the preset division ratio (8 to 16,383) of the 14-bit programmable reference counter. The guaranteed maximum allowable input frequency to the reference counter is 10 MHz; f_{MAX} to the swallow counter and 10-bit programmable counter is 17 MHz.

GaAs provides fast division

Unlike a PLL, a prescaler has no onboard oscillator, but instead uses the incoming signal to drive flip-flops and other logic circuits. The prescaler generates an output whose frequency is a submultiple (determined by the number of flip-flops and the arrangement of the feedback logic) of the input frequency.

To effect frequency division at frequencies higher than 1 GHz, you can use GaAs sequential- and combinatorial-logic blocks to make prescalers. To avoid some of the headaches associated with connecting these UHF elements together, though, you might do well to consid-

For more information . . .

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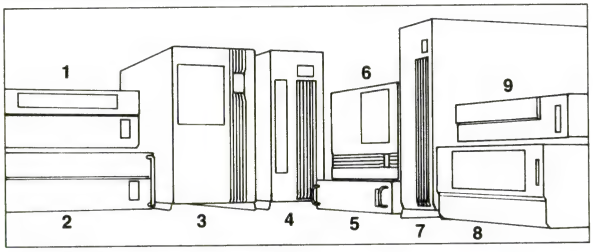

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er using ready-made GaAs frequency-division blocks, such as some recently announced parts from Harris Microwave Semiconductor and GigaBit Logic.

Model HMD-11011-2 from Harris is a divide-by-10/11 element that accepts input frequencies as high as 2 GHz. The device is suitable for use in programmable pulse-swallowing counters, microwave communication systems, satellite-receiver systems, microwave instrumentation, and high-speed video processing.

A single mode-control input sets the division ratio to 10 or 11; the IC divides by 10 when this line is high, by 11 when low. All I/O lines are ECL compatible. Typical propagation delay through the HMD-11011-2 is 950 psec. The IC is designed to operate over −55 to +125°C, in a 50Ω system. It costs $241 (100).

Fig 5 shows an application circuit in which the HMD-11011-2 works in conjunction with Harris's $117 (100) HMD-11301-2 divide-by-2 device, to perform a progammable divide-by-20 or -22 operation. Although the devices' specs guarantee that this circuit will operate with input frequencies as high as 2 GHz, Harris reveals that tests show the configuration is valid for frequencies as high as 2.5 GHz.

Multiply by *n* using GaAs

The preceding section described the use of GaAs ICs in a fixed-modulus (20 or 22) frequency-division application. By using GaAs devices in a variable-modulus-divider configuration in conjunction with a PLL, you obtain quite the opposite results: multiplication of an input frequency by a selectable factor.

Fig 6a's block diagram shows how to use GigaBit Logic's 10G061 pro-

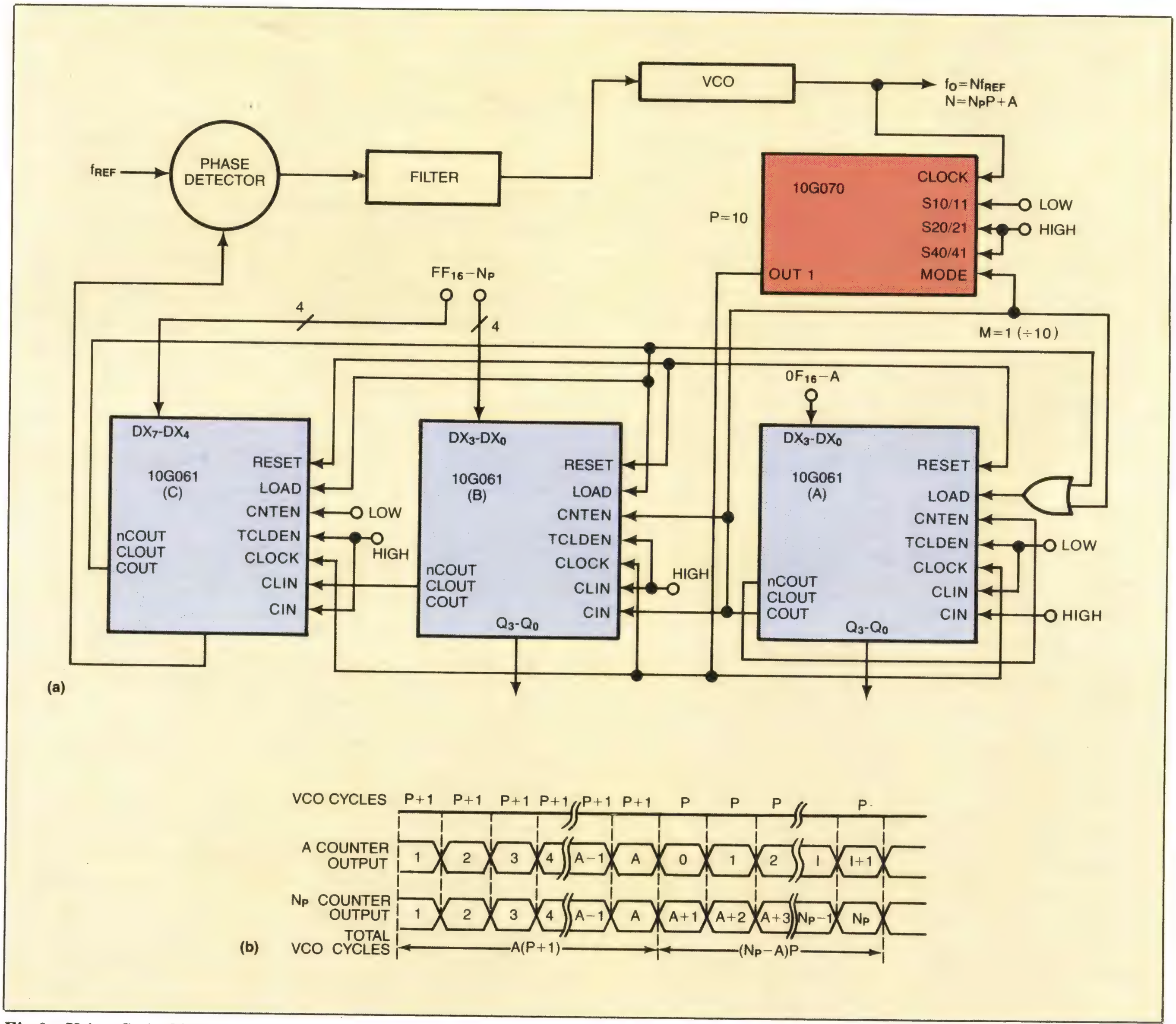

Fig 6—Using GaAs ICs in a synthesizer application, *this circuit produces an output frequency that's an exact, programmable multiple of the input reference frequency. Programmable output frequencies can reach 2 GHz. The 10G061 and 10G070 ICs, from GigaBit Logic, serve as programmable counters and a prescaler, respectively. The VCO cycles and counter outputs are shown in* ***b.***

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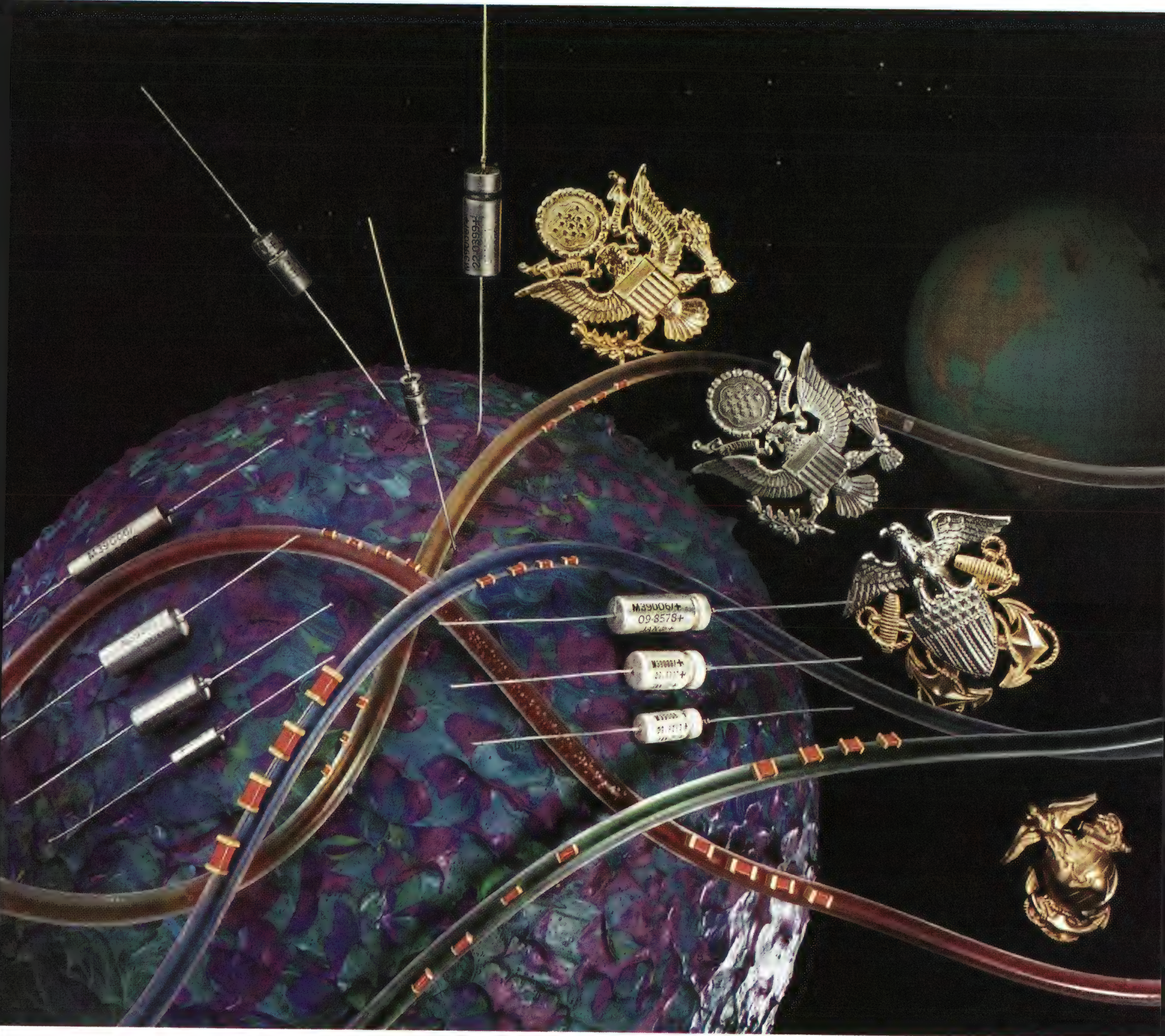

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grammable counter and 10G070 variable-modulus divider to make a programmable frequency synthesizer. The two ICs make up a swallow counter. Prices for the 10G061 and the 10G070 (1.5-GHz grade) are \$99.50 and \$129 (100), respectively.

The 10G070 variable-modulus divider initially operates in the ÷(P+1) mode. The IC strobes the A and N_P counters every P+1 cycles of the VCO's output signal. When the A counter overflows, it sets the variable-modulus divider to the ÷P mode. The VCO cycles are shown in **6b**, and the resulting output frequency is

$$f_{OUT}=(A(P+1)+(N_P-A)P)f_{REF}$$

or

$$(A+N_P P)f_{REF}.$$

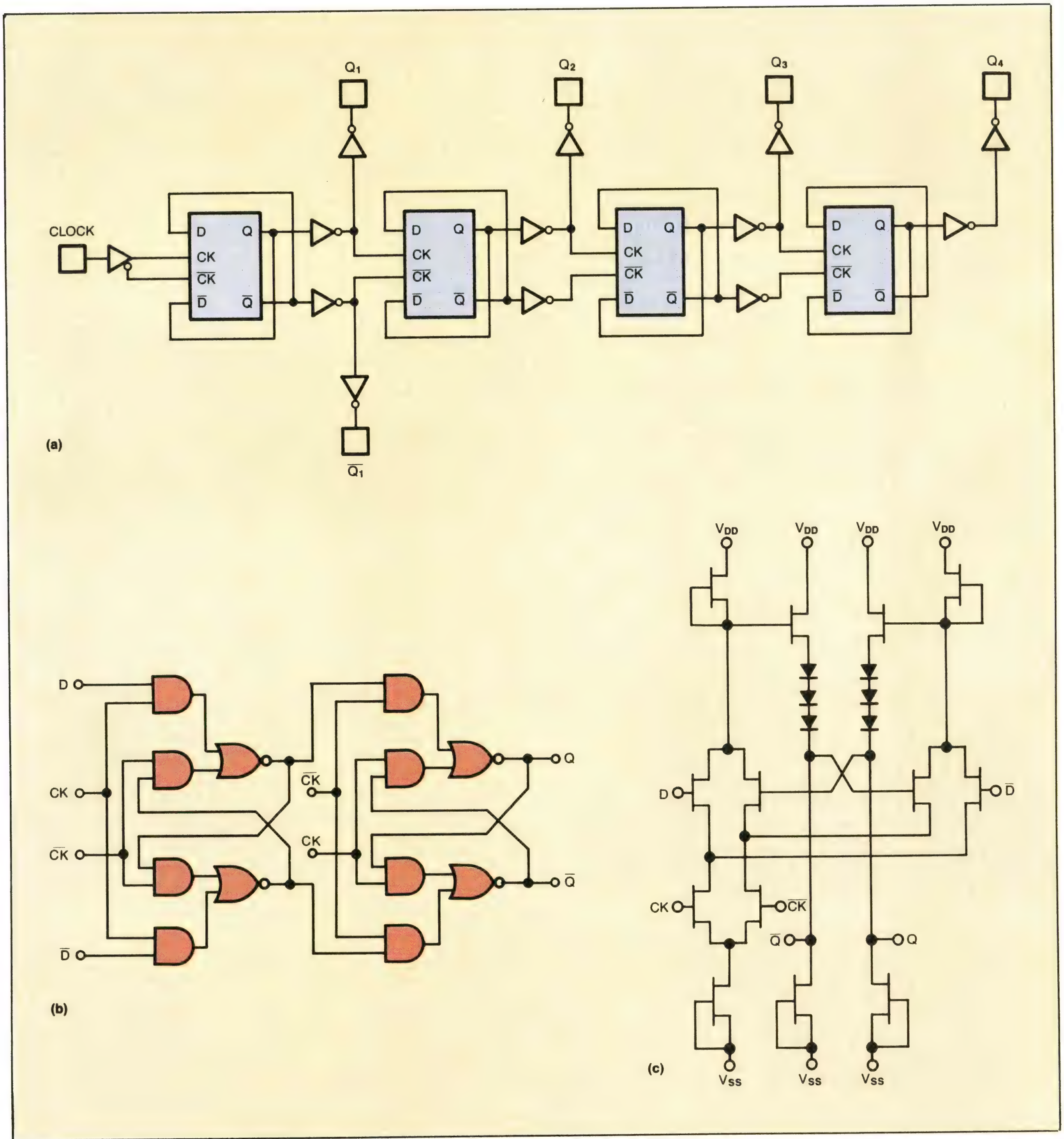

Fig 7—This GaAs-processed, combined custom/semicustom 4-bit prescaler *from TriQuint Semiconductor uses both standard cells and custom cells. The custom-developed flip-flop cell in c provides better characteristics than the flip-flop in* ***b,*** *which is constructed from standard logic cells. The prescaler accommodates input frequencies as high as 3.3 GHz.*

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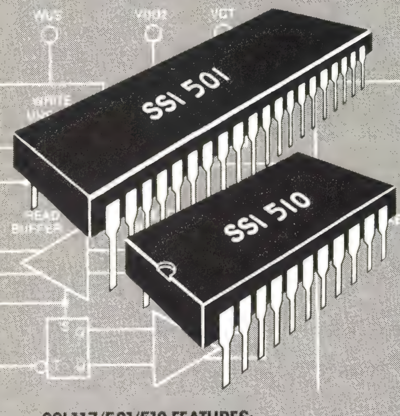

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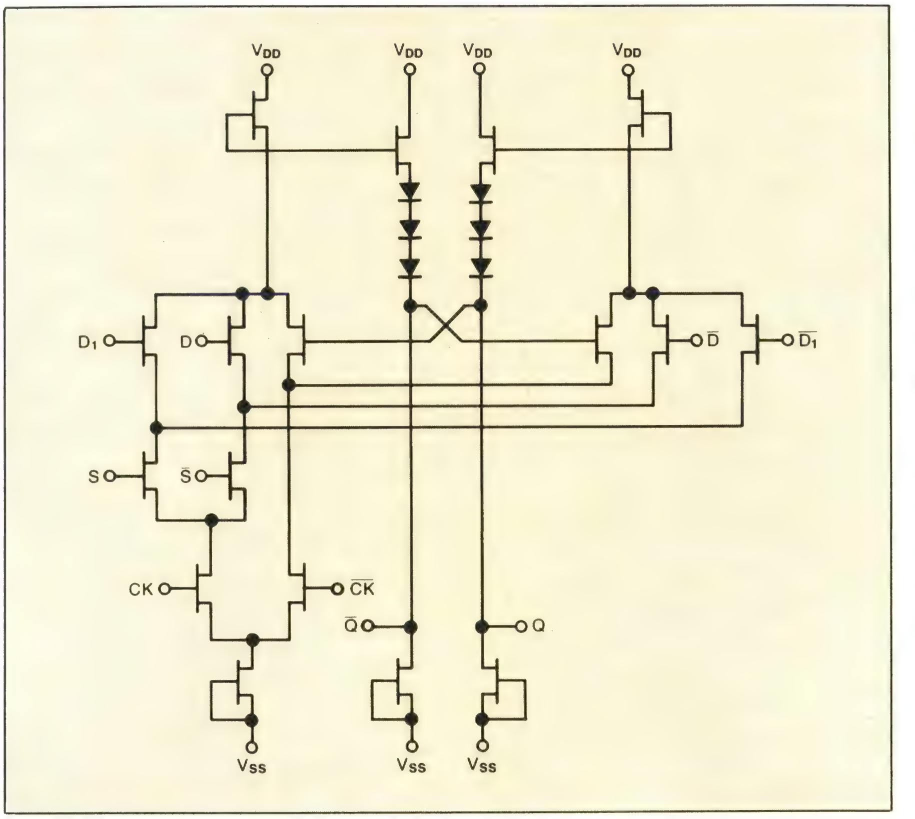

Fig 8—A custom-built, multiplexed flip-flop provides 3-level gating *in a GaAs-processed semicustom/custom modulus-4/5 divider developed by TriQuint Semiconductor. The divider requires flip-flops having multiplexed inputs. The custom flip-flop shown here introduces less delay than you'd obtain using a flip-flop made from the company's standard-cell logic cells.*

In the example shown in **Fig 6,** you can set the coefficient A to any value from 1 to 15, and N_P to any value from 1 to 255. P is 10. The maximum output frequency of the synthesizer is set by the 10G070's clock-rate limit: 1.25, 1.5, 1.75, or 2 GHz, depending on the device you select.

All the GaAs frequency-control ICs described thus far are standard catalog items. If your system has particular frequency-division requirements, however, a custom or semicustom GaAs device might be more appropriate for the application. TriQuint Semiconductor, for example, offers a family of custom and semicustom GaAs circuits that use a buffered-FET logic block.

Elements in TriQuint's GaAs cell library include NOR gates and other logic functions. I/O cells include ECL interfaces, as well as TTL and CMOS translation circuits. Two frequency-control circuits described at last May's Custom Integrated Circuits Conference in Rochester, NY, illustrate the possibilities of designing with GaAs custom/semicustom ICs.

The 4-bit (÷2, 4, 8, 16) prescaler shown in **Fig 7** requires extremely high-speed flip-flops. The flip-flop in **7b** uses elements from the standard-cell library. However, the full-custom flip-flop shown in **7c** uses a differential pair to implement its logic, and it thereby yields a higher speed than the standard-cell block. Tests show that the 4-bit prescaler can accept input frequencies as high as 3.3 GHz.

Another example of the use of GaAs custom/semicustom ICs for frequency division is a modulus-4/5 divider. Such a divider requires flip-flops that have multiplexed inputs. Again, standard-cell gates could implement the flip-flops, but they

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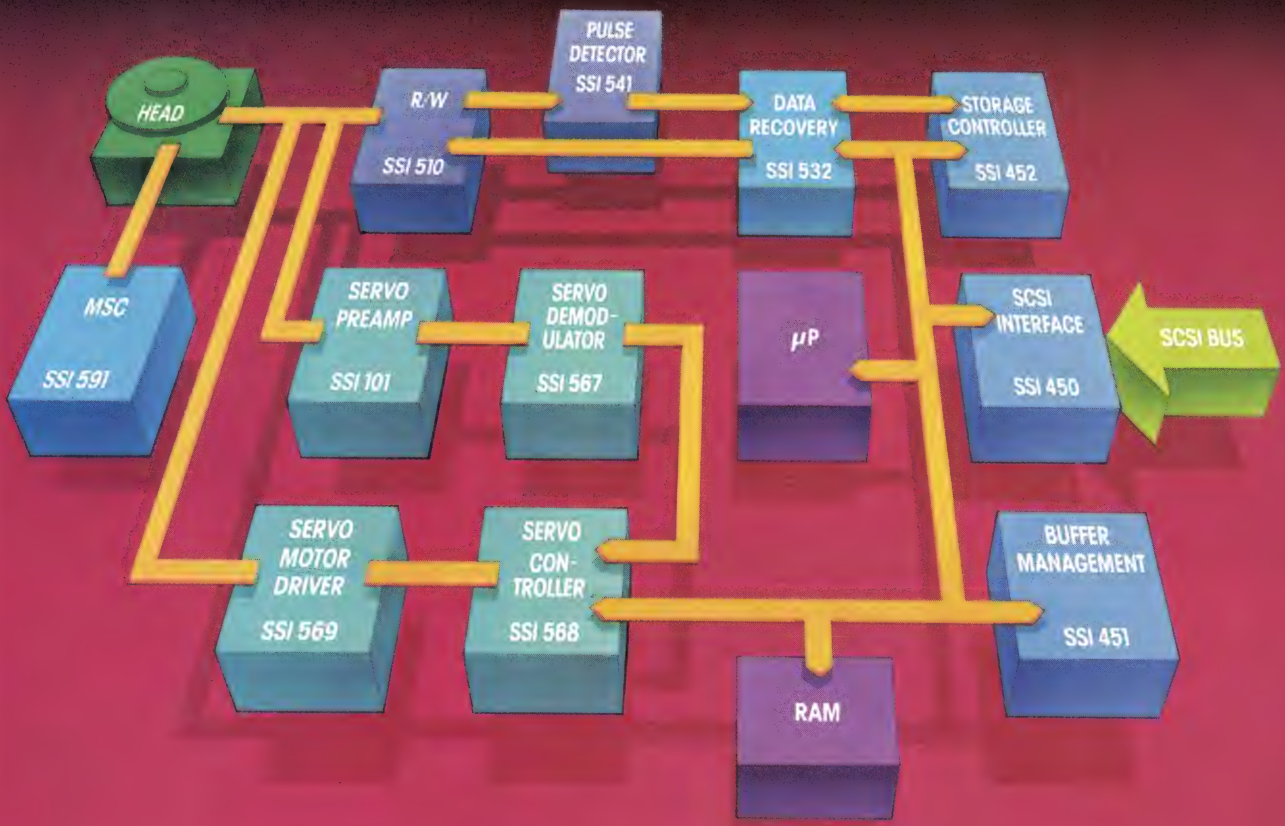

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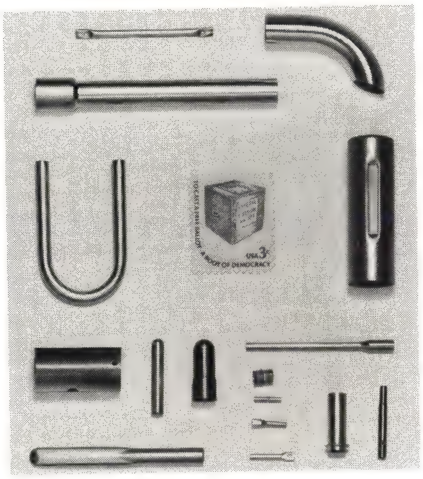

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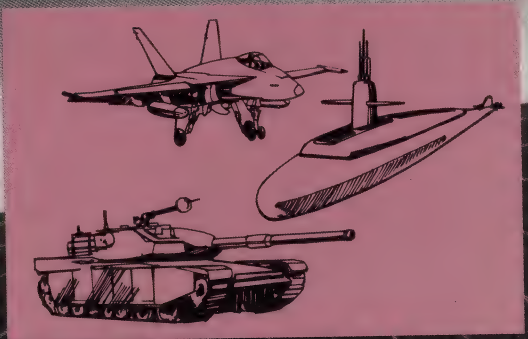

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would introduce an extra delay in the feedback path.

A custom cell again comes to the rescue. The multiplexed flip-flop in **Fig 8** incorporates the gating needed by the divider; an additional differential pair at the flip-flop's input provides a third level of gating. The IC's buffered-FET logic can drive the flip-flop's select and data inputs, but the clock inputs require drive levels approximately one diode drop lower in order to maintain adequate noise margins. Test results show that the 4/5 counter accommodates clock frequencies as high as 2.5 GHz.

Using custom cells in these frequency-control circuits involves a tradeoff in the form of additional design and layout time. However, for such MSI devices, the layout time is not a great deal more than that required for standard-cell parts. And the benefits afforded by the custom circuitry can be significant: For the 4-bit prescaler, for example, the combination custom/standard-cell design (in which 30% of the IC's cells are custom circuit blocks) exhibits a 50% speed improvement over the version that uses standard cells exclusively.

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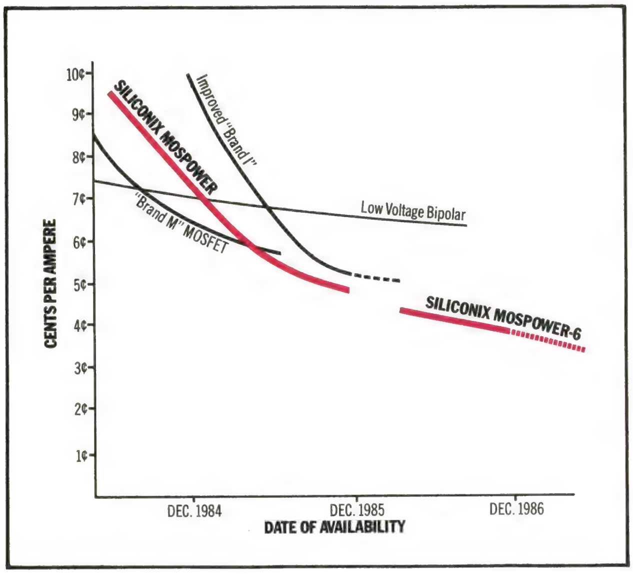

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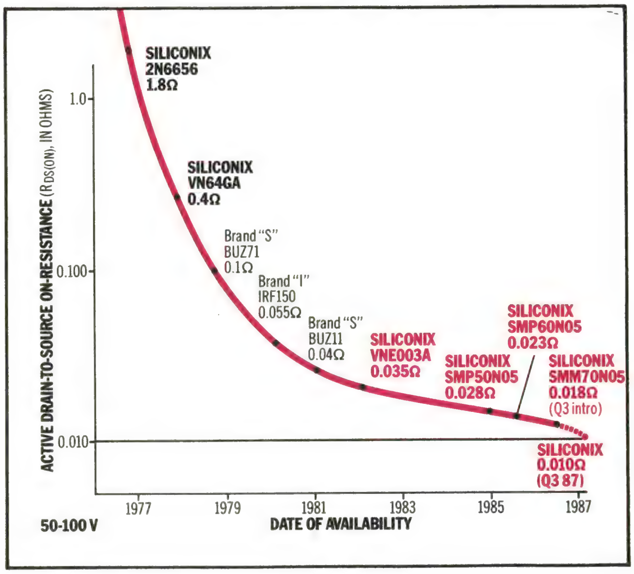

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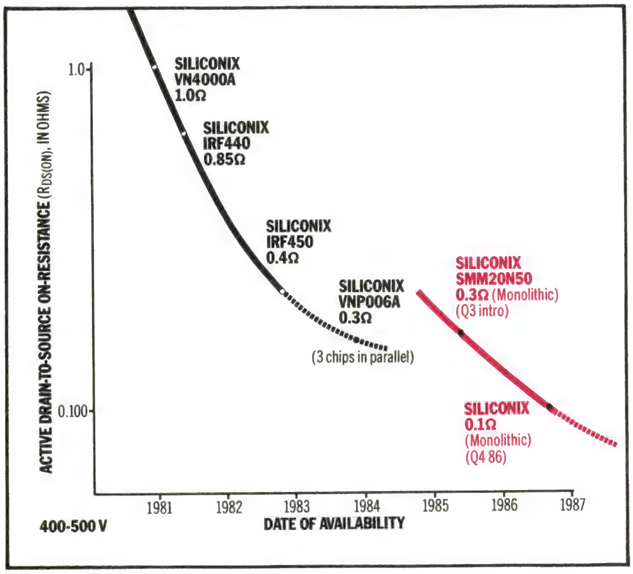

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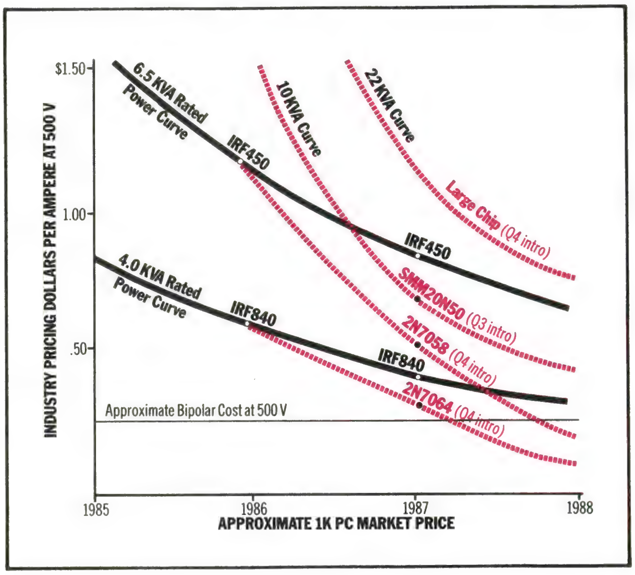

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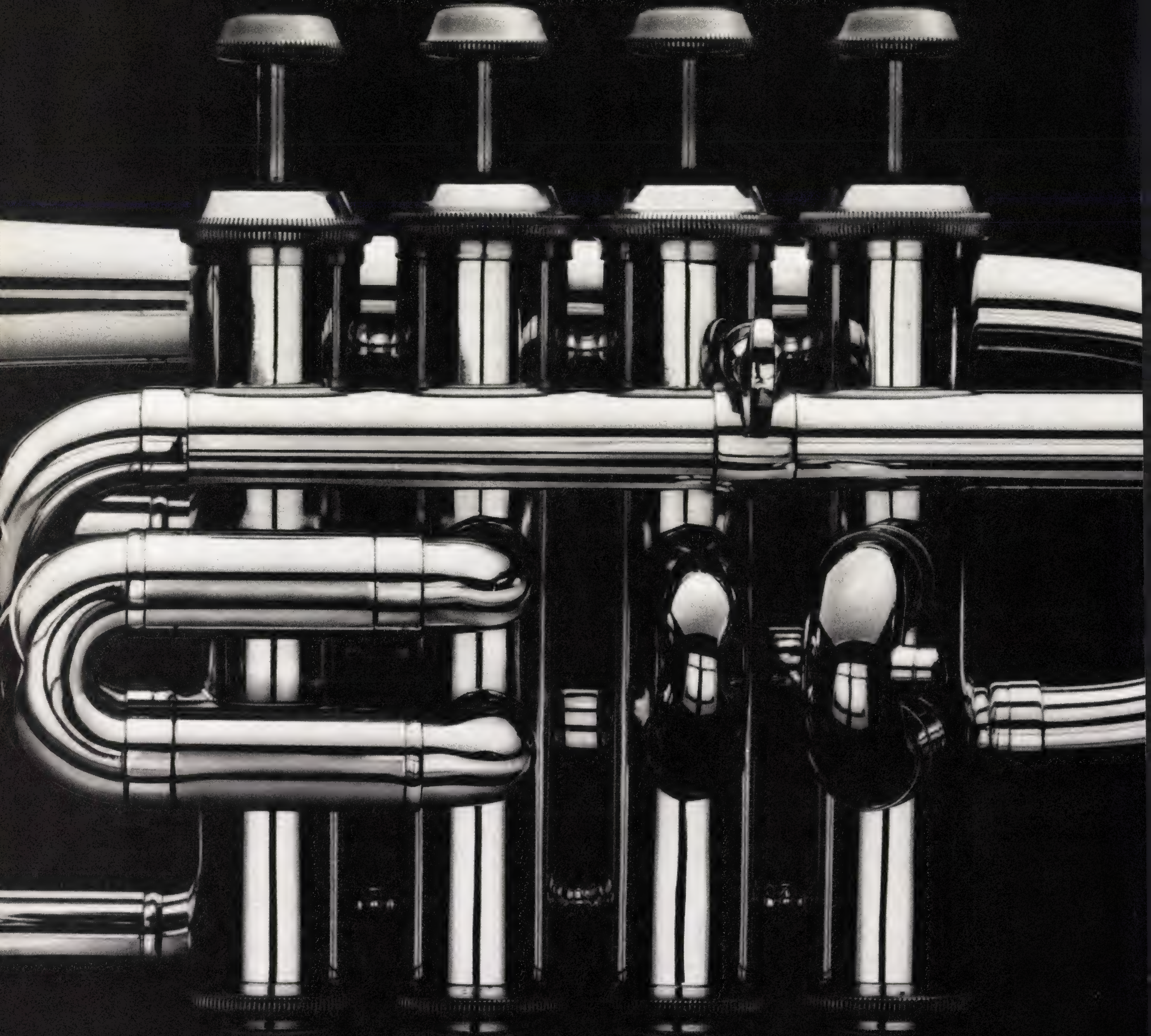

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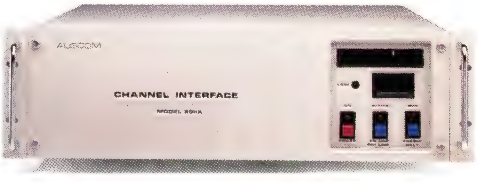

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TECHNOLOGY UPDATE

Multiprocessor computers execute tasks in parallel for faster performance

Chris Terry, *Associate Editor*

These 32- and 64-bit array processors, *which make up CSPI's Maxim Series, supplement a MicroVAX II. You can obtain one in either a stand-alone cabinet or housed with the MicroVAX II host computer in a desk unit.*

It's been 14 years since the University of Illinois developed the first massively parallel computer (Illiac IV) and had it installed at NASA's Jet Propulsion Labs. In the intervening years, research into the hardware and software problems of parallel processing has continued at all levels, and although problems and unfortunate tradeoffs linger, it's now possible to link inexpensive processors to yield the performance of a supercomputer at a fraction of the cost of an equivalent uniprocessor.

In the last two years, many parallel computers with widely different architectures have appeared. Still, you can divide them roughly into three classes, depending on their degree of granularity, or the level of software complexity at which tasks are divided between the available processors for concurrent execution. Large-grain machines have from two to 32 processors, which share global memory (though they may have local memory as well). There are two types of fine-grain parallel computers. Some are configured so that each processor executes the same instruction on a different data stream (also called single-instruction, multiple-data, or SIMD, machines). Finally, another type of fine-grain machine has each of its processors execute different sections of code on different data streams, passing data, commands, and messages to other processors over a communications network. These are also called multiple-instruction, multiple-data (MIMD) machines.

Large-grain machines have only a few processors, each of which can independently execute quite large sections of code; they communicate with each other via global memory, although each one may also have some local memory to serve as work space. You can, indeed, assign a separate application program to each processor, or you can accelerate each individual program by executing some of its tasks concurrently, as well as executing the overall job stream concurrently. This flexibility in assignment is one of the important advantages of large-grain machines, but not all programs lend themselves to concurrent execution.

Another important advantage of large-grain machines is that programming them is relatively easy. Generally, you use an optimizing compiler to detect sections of code that lend themselves to parallel execution (DO loops are a typical example). The optimizing compiler is machine-specific and inserts into the compiled code the instructions that assign sections of code and the related data to the individual processors; some machines use dedicated hardware to execute the assignment instructions. Optimizing concurrent compilers are usually available for Fortran, C, and Pascal, and you can often recompile an existing application program for concurrent execution with little or no modification of the original source code.

In general, large-grain parallel machines provide modest accelera-

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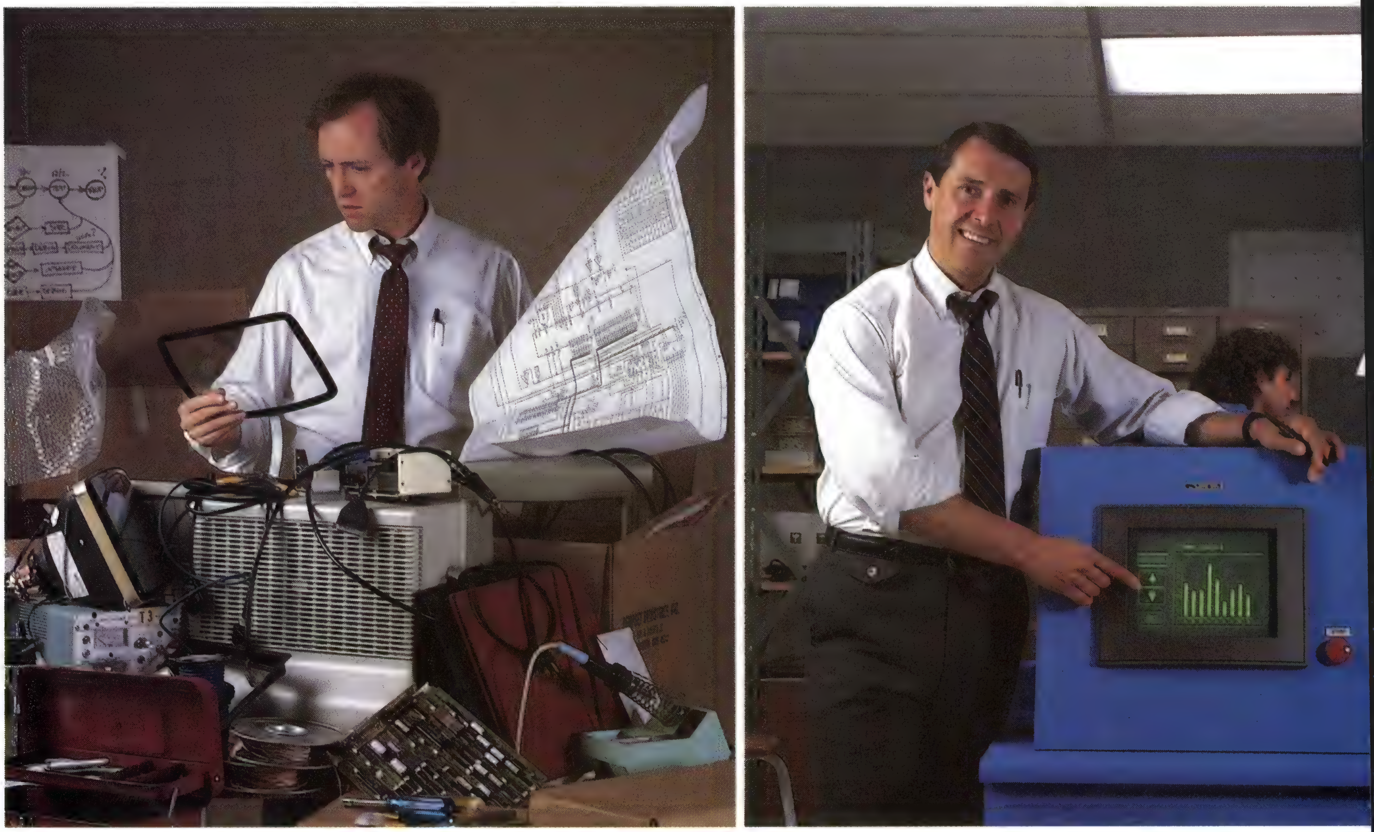

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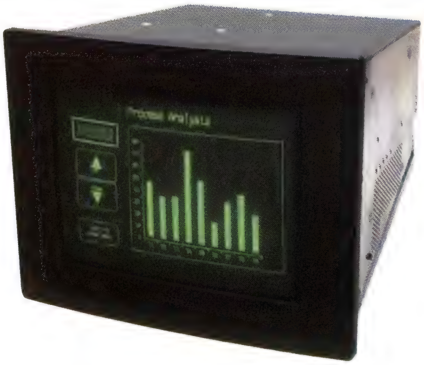

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tion (two to five times) for a wide variety of applications. Further, very little software effort is needed to take advantage of their capabilities; thus, they are cost effective in terms of both hardware and software.

Eight processors are possible

Typical machines in this class are the Alliant FX/8 and the Sequent Balance 21000. The Alliant machine uses as many as eight processors, linked by a concurrency-control bus as well as by global memory. Interactive processors, running in parallel with the computational processors, maintain system response for interactive users even when the computational processors are fully loaded. The Sequent Balance 21000 can have as many as 30 32-bit processors, which communicate with each other via global memory and special synchronization hardware.

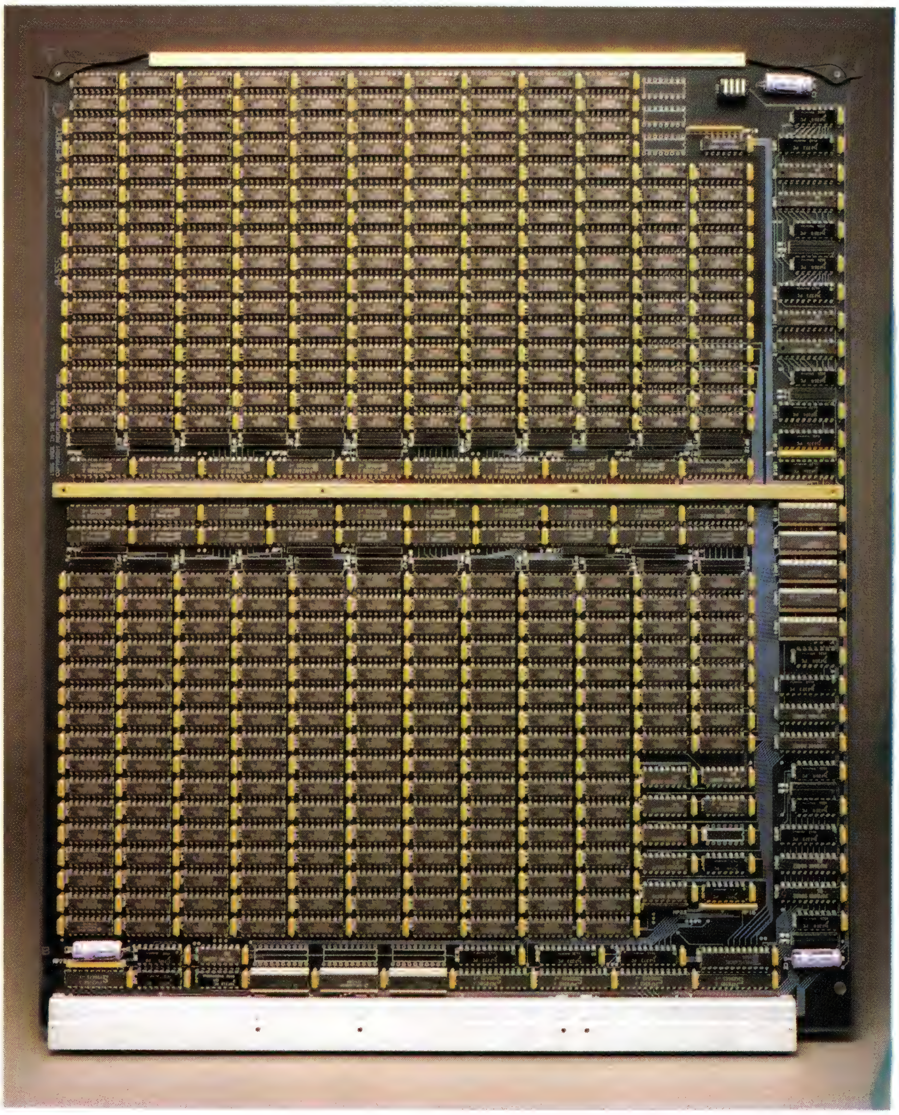
The Culler 7 family of machines falls into the large-grain class because they have only a few processors and exploit opportunities to run large sections of code concurrently. Internally, however, the user processors (which perform most of the computational work) make extensive use of fine-grain techniques to exploit all possible parallelism in the execution of primitives. The machines use a conventional Von Neumann architecture in the kernel processor to establish tasks and distribute them to the user processors and can therefore run any software that runs on a Cray machine.

The family provides sustained execution of 4M to 16M flops, depending on whether you configure the system for one, two, three, or four of the vendor's 64-bit processors. The kernel processor, running a Unix-compatible operating system, communicates with workstations via an Ethernet bus and with shared resources via a Multibus. A system-control interface, operating under control of the kernel processor, allows any Multibus device to access global memory and performs block transfers of data between devices and memory or between blocks of memory.

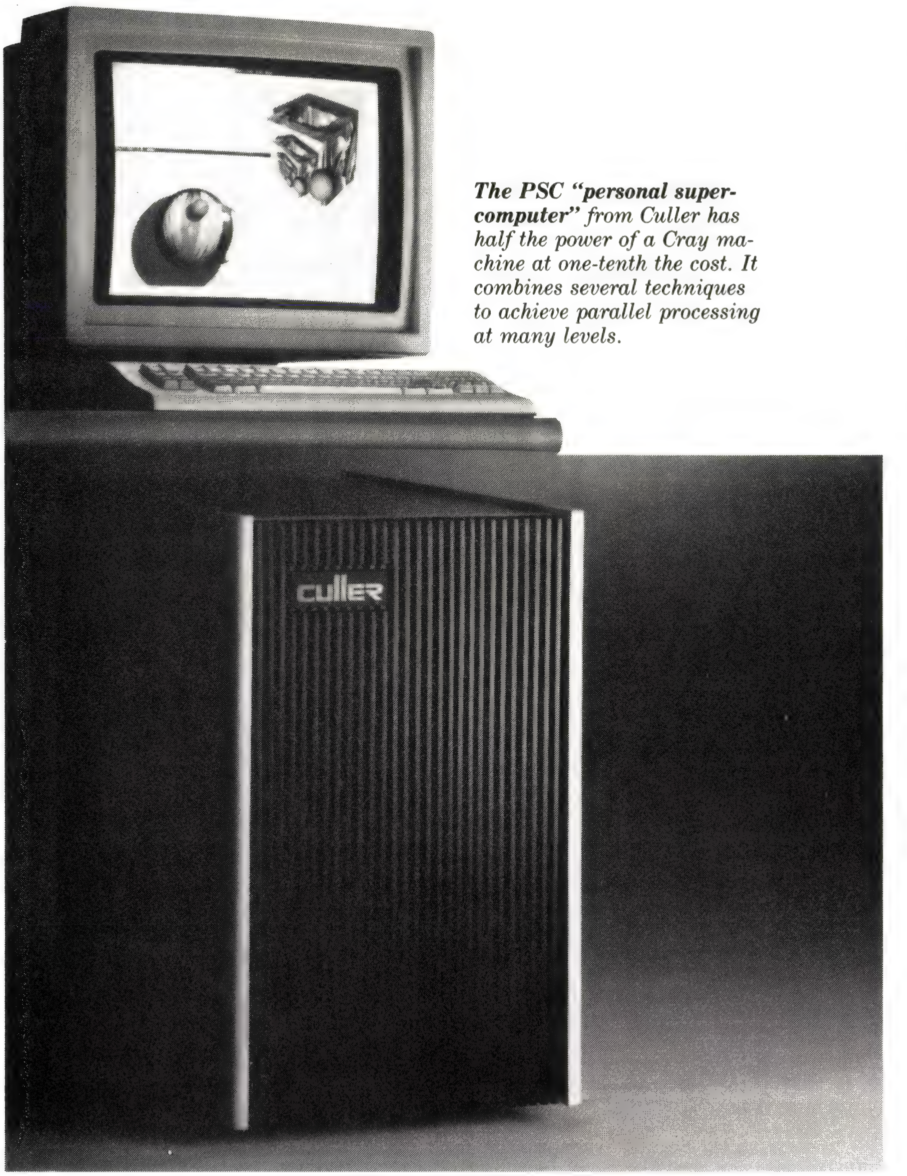
A special staging bus allows the transfer of data between global memory and any of the four (max) user processors. These processors each consist of a P machine (local memory and sequencing facility), an A machine (32-bit integer processor), an XY machine (integer and floating-point processor), and local memory.

Array processors are an example of fine-grain, memory-based machines with a restricted set of simple instructions and are generally dedicated to numeric computations on data passed to them by a general-purpose host computer. The data word is usually 32 or even 64 bits wide, so that even quite complex operations take few clock cycles.

All processors in an array processor execute the same instruction at any given moment, but on different data sets. The vendor usually provides ROM-resident primitives to perform the arithmetic functions and a software interface that allows the host to call the desired primitives from an applications program written in Fortran or other high-level language (HLL). Quite often the vendor also supplies an HLL



This general-purpose accelerator*—the Compute Engine from Mentor Graphics—includes six function processors and as much as 20M bytes of memory. It incorporates concurrency of functions at the instruction-execution level.*



The PSC "personal supercomputer" *from Culler has half the power of a Cray machine at one-tenth the cost. It combines several techniques to achieve parallel processing at many levels.*

library of subroutines to perform more complex mathematical operations.

Array processors can increase execution speed by a factor of 20 or more and are relatively easy to program, but their usefulness is limited to numeric computations that perform the same operations iteratively on many different sets of data.

Representative of array processors is CSPI's Maxim Series. The series is available in 32- and 64-bit configurations that operate in conjunction with a MicroVAX and perform matrix operations at rates of 5M flops, whereas a MicroVAX alone could perform the same matrix operations at no more than 0.5M flops. Other array processors are available for host computers of all sizes, including several that plug into an extension slot in an IBM PC or compatible **(Ref 1).**

Array processors are specialized for certain types of data-processing problems, but not all fine-grain machines are so restricted. The Mentor Compute Engine is a general-purpose accelerator for CAE workstations and can maintain an execution rate of 8M flops over a spectrum of tasks.

This accelerator combines several different techniques to achieve its performance. The CPU is based on a reduced-instruction-set computer architecture and employs a number of functional processor units, each controlled by a field in the 64-bit instruction word, to perform low-level functions in parallel. The processors include two arithmetic and logic units, register control units, address generators, and memory control units for as much as 20M bytes of dedicated memory.

The Compute Engine bus allows data transfers between the processor units and local memory at speeds as high as 32M bytes/sec. Communication between the Compute Engine and the host workstation takes place via a high-speed, buffered, bidirectional DMA channel.

The vendor provides a comprehensive set of software development tools that allow you to develop application programs to capitalize on the low-level parallel-processing capabilities of the machine. The optimizing compiler not only detects high-level constructs suitable for parallel execution but also adapts in-line code to take advantage of the parallelism inherent in the machine's low-level primitives.

Another type of MIMD machine divides its tasks among a large number of general-purpose μPs, each of which has its own memory and executes multiple instructions to complete its assigned task. The μPs communicate with each other either over a fast bus that includes a switching network, or by passing messages over a separate communications channel.

Because μPs are inexpensive, it has long been a designer's dream to interconnect them in numbers so large that their combined computing power would outperform a mainframe. The Intel iPSC family, introduced in 1985, is based on the California Institute of Technology's hypercube topology and provides as many as 128 Intel 80286 μPs, each directly connected to all the others to form nodes of a multidimensional cube.

The processing element at a node consists of an 80286 CPU with an

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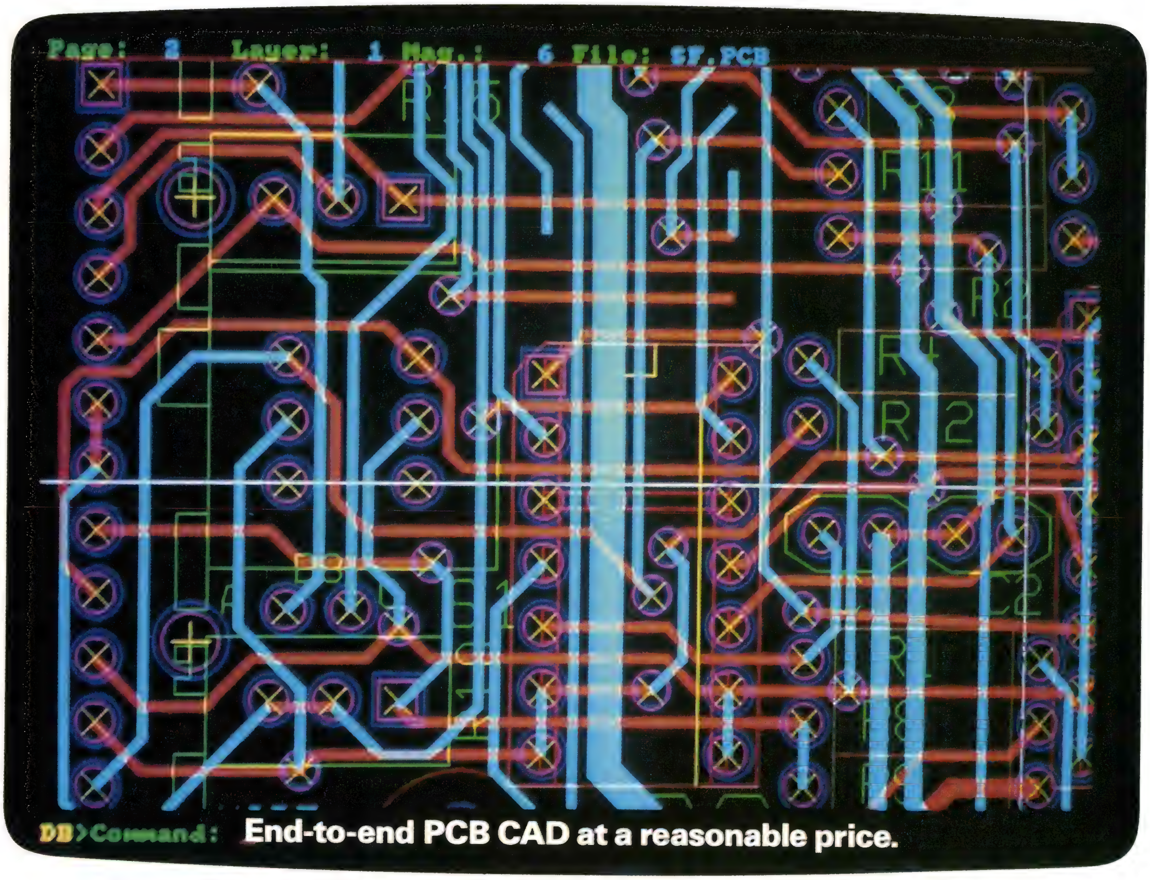
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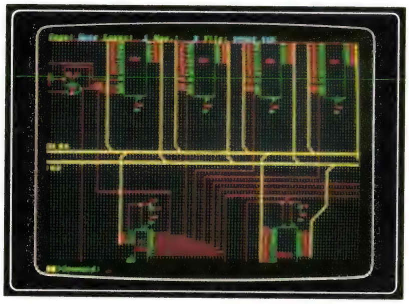

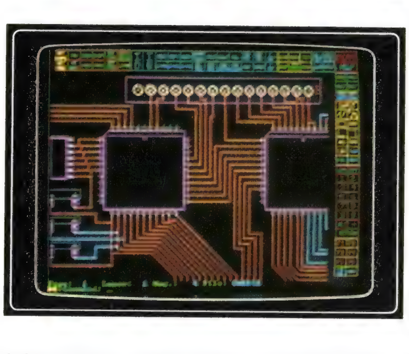

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80287 math coprocessor, a 512k-byte dual-port memory, and eight 82586 communications coprocessors. Seven of these handle interprocessor communications; the eighth provides a global Ethernet channel to the cube manager (also based on the 80286) for program loading, data input and output, and diagnostics.

Software consists of a PROM-resident monitor on each node board and an operating-system kernel that's downloaded from the cube manager into RAM after initialization. This kernel provides cube-wide facilities for message-passing between nodes. The cube manager runs the Xenix operating system, to which Intel has added facilities that dynamically assign processes or tasks to each node.

The more recent iPSC-VX family members include a vector processor at each node and provide a Fortran program-development system within the context of the Xenix operating system. The iPSC machines yield performances of 10M flops (or more); the iPSC-VX machines perform 100M to 200M flops.

The Ametek System 14 also uses the hypercube topology, and the vendor offers configurations with as few as 16 to as many as 256 node processors. Each node consists of an 80286/80287 computational processor and an 80186 I/O processor for internode and global communications. You can use the system in conjunction with a cube manager consisting of a VAX 11/780 or a MicroVAX II. Performance ranges from 0.8M flops for a 16-node cube to 12M flops for a 256-node cube. Like the Culler 7 machines, these machines use a Von Neumann cube manager that simplifies the adaptation of existing applications software and the development of new software for the machine.

Hybrids are possible

The Butterfly computer, from BBN Advanced Computers, can have as many as 256 processor nodes, each consisting of a 68020 CPU, a 68881 math coprocessor, a VLSI processor node controller (PNC), and a maximum of 4M bytes of memory. The PNCs provide a fast packet-switching network that allows any processor to access the memory of any other processor and to store or retrieve data there within 120 nsec.

This network causes the Butterfly to exhibit some of the characteristics of a hypercube machine, in that each processor can operate indepen-

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dently, using its own memory. This network also causes the computer to show some of the characteristics of an array processor, in that all of the local memories combine to act as a global, shared memory. Thus, the machine can exploit parallelism both at the source-code level and at the primitive level of operation. The vendor provides an operating system and software development tools that let you develop programs in a manner that allows for optimum performance for a particular application.

Each of these three classes of architectures has both advantages and disadvantages, and so potential users of such machines must consider quite complex tradeoffs. An example of such a tradeoff involves the relative importance of turnaround and throughput for your application. Turnaround is the time required to complete a single job; throughput refers to the average completion time for multiple jobs in a stream.

If the architecture of your parallel computer is optimized for a particular type of problem, then the turnaround for jobs of that type may show an improvement of a factor of 20 or more. However, turnaround for jobs not related to that problem may show little or no improvement over the turnaround on a uniprocessor, so that the improvement in overall throughput may be no more than two or three times. A different type of architecture might yield a throughput improvement of four or five times, regardless of the type of problem involved. Obviously, the nature of your applications will influence your choice of architecture.

Regardless of which type of parallel computer your applications call for, almost all the software currently available is based on the serial nature of the Von Neumann architecture, which assumes that the computer will execute instructions in a fixed order, one after another. HLLs and their older compilers make the same assumption. At present, even highly parallel architectures such as those based on the hypercube continue to use the Von Neumann model within each node.

Thus, the problem of software development remains. The hypercube topology (and possible future hypercube types of approaches) seems to offer the best potential for cost-effective general-purpose machines that will provide performance equaling or exceeding that of current uniprocessor supercomputers. However, such parallel-processing computers will require a long and intensive software development effort to make the most of their capabilities.

Current computational algorithms assume serial execution and may not be adequate for parallel machines; much work on algorithms is currently in progress both at Caltech and at MIT. Other problems relate to the distribution of tasks to the various nodes in such a way as to balance the workload and to ensure that nodes do not become overloaded or idle.

For now, the factors that will primarily govern your choice of hardware are those pertaining to immediacy and economics. For a narrowly focused application, such as graphics processing, a dedicated, fine-grain engine may meet your needs provided that it has an adequate HLL interface to facilitate software development. If your needs are broader, but a modest acceleration over a wide range of tasks will suffice, one of the large-grain machines with an optimizing compiler may meet your needs and budget and minimize software development problems. **EDN**

Reference

1. Tetewsky, Avram K, "Accelerate your PC's arithmetic with an array processor," *EDN*, October 3, 1985, pg 155.

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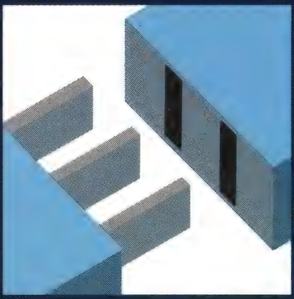

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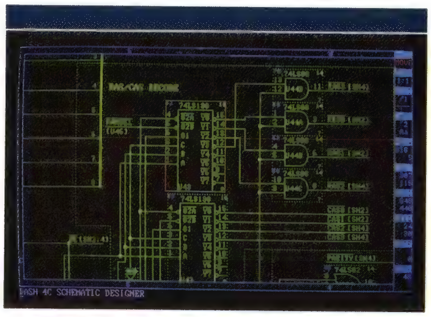

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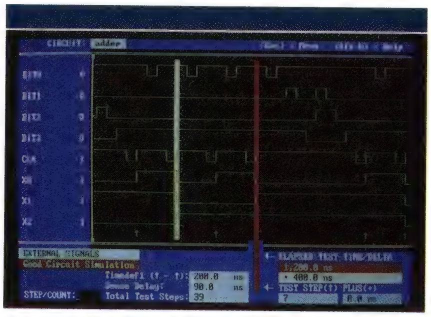
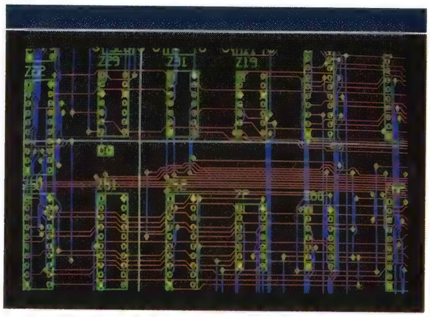


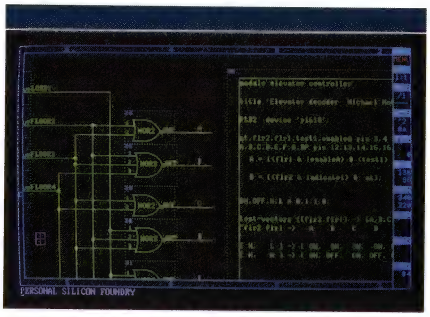
DASH-CADAT PLUS: SIMULATE LOGIC, TIMING AND FAULTS WITH THE POWER OF A MAINFRAME.

- Logic simulation up to 30,000 gates
- Fault simulation for full testability
- Rivals mainframe performance
- Display processor operates like a logic analyzer
- Stimulus language simplifies test vector generation
- Simulates at transistor, gate, functional or behavioral level
- ASIC libraries and optional hardware modeler



DASH-PCB: LAY OUT PCBs FOUR TIMES FASTER THAN THE EXPERTS.

- Expert multi-strategy router
- Trace hugging frees maximum number of routing channels
- Real-time rubber banding optimizes component placement
- Automatic 45 degree routing
- Board capacity up to 32″ X 32″
- Design rule checking ensures accuracy
- Multiple trace layers to handle the most complex designs



PERSONAL SILICON FOUNDRY: CONCEPT TO SILICON IN THREE HOURS.

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CIRCLE NO 57

Graphic proof of high-tech leadership.

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fx-7000G GRAPHICS
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TEXAS INSTRUMENTS TI-30 SL
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SHARP

The Casio fx-7000G $79.95 It's the world's first programmable scientific calculator with a graphic display. The only calculator that can give form to your figures, instantly drawing graphs that represent your formulas and calculations on its big LCD screen.

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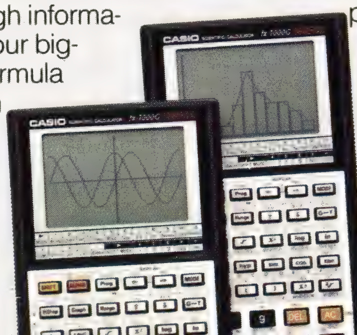
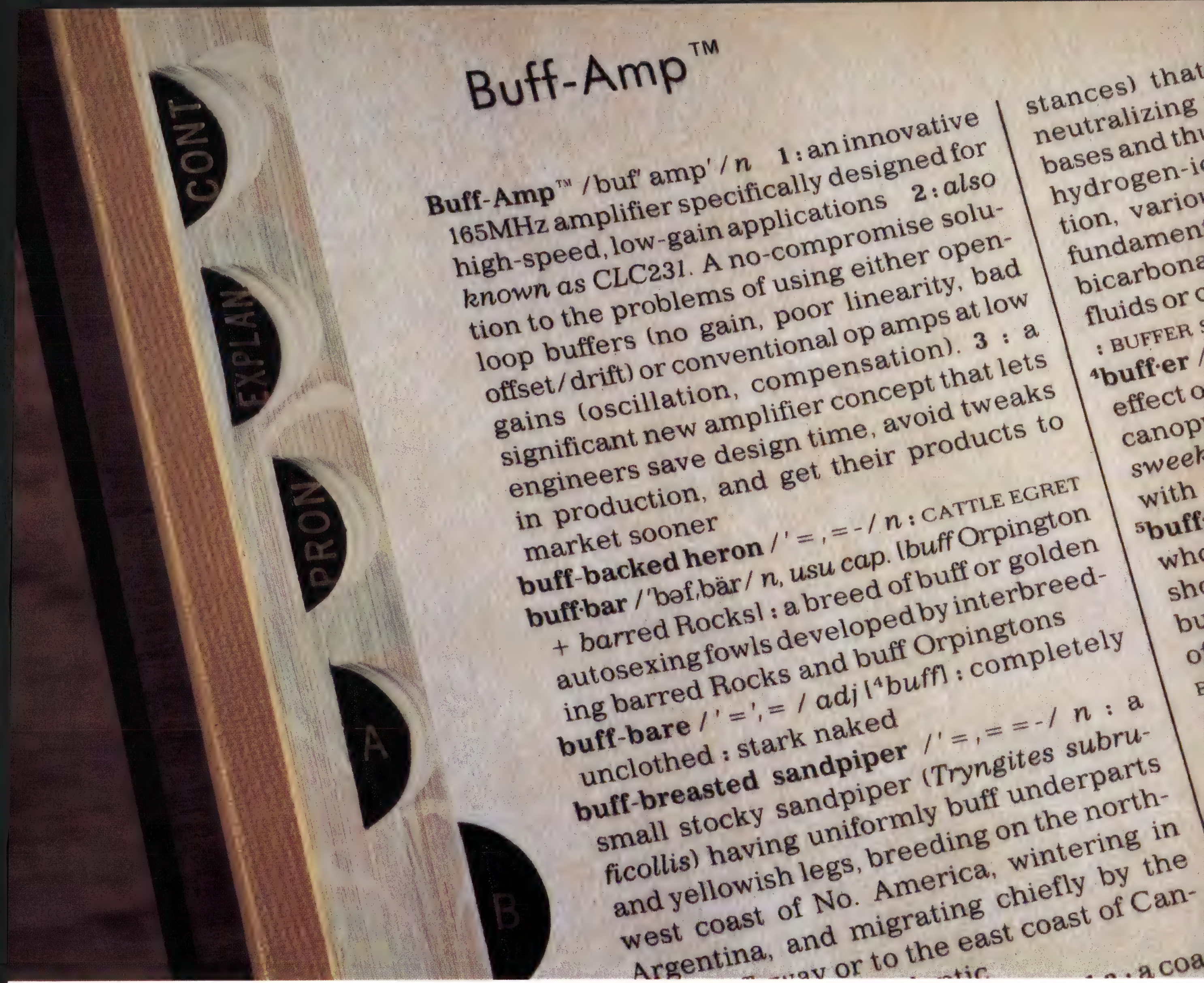
CIRCLE NO 58





Buff-Amp™

Buff-Amp™ /buf' amp'/ *n* **1**: an innovative 165MHz amplifier specifically designed for high-speed, low-gain applications **2**: *also known as* CLC231. A no-compromise solution to the problems of using either open-loop buffers (no gain, poor linearity, bad offset/drift) or conventional op amps at low gains (oscillation, compensation). **3**: a significant new amplifier concept that lets engineers save design time, avoid tweaks in production, and get their products to market sooner

buff-backed heron /'=,=-/ *n*: CATTLE EGRET

buff·bar /'bəf,bär/ *n, usu cap.* [*buff* Orpington + *barred* Rocks]: a breed of buff or golden autosexing fowls developed by interbreeding barred Rocks and buff Orpingtons

buff-bare /'=',=/ *adj* [⁴buff]: completely unclothed: stark naked

buff-breasted sandpiper /'=,==-/ *n*: a small stocky sandpiper (*Tryngites subruficollis*) having uniformly buff underparts and yellowish legs, breeding on the north-west coast of No. America, wintering in Argentina, and migrating chiefly by the east coast of Can-

stances) that
neutralizing
bases and th
hydrogen-i
tion, vario
fundamen
bicarbona
fluids or c
: BUFFER
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effect o
canop
sweek
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How to enrich your high-speed, low-gain vocabulary in 30 seconds or less.

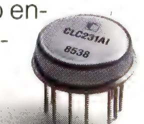
Once you've gleaned the meaning of Buff-Amp,™ you'll know how to get the best features of high-speed op amps and high-performance buffers. From a single device!

With Buff-Amp,™ you get gains from ±1 to ±5 without sacrificing the 165MHz -3dB bandwidth. Linearity that is a true 0.1%, even with demanding 50 ohm loads. A 1mV input offset and 10μV/°C drift. *Plus* freedom from oscillation across the entire gain range…without compensation.

There's nothing academic about the specs of Buff-Amp™ in real-world operation at the system level. You can be sure of a 95MHz full power bandwidth. A 15ns settling time to 0.05%. A 100mA output current. A 3000V/μs slew rate. A 2.0ns rise time. And, in many designs, the ability to operate on ±5V and 5mA—just 50mW of power. That's unabridged performance in anyone's book!

Buff-Amp™ is the astute choice for tasks such as driving flash A/Ds or matched lines, or buffering current-output DACs, in EW, ATE, and other applications.

Now that you've taken 30 seconds to enrich your high-speed, low-gain vocabulary, take a few more and call or write us for complete literature. Comlinear Corporation, P.O. Box 20600, Fort Collins, CO 80522, (303) 226-0500.



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CIRCLE NO 61

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Carroll Touch offers a line of high-performance, cost-effective infrared touch systems and EL displays equipped with touch. Providing exceptional functionality and exceptional flexibility, these MIL SPEC-qualified units make user interaction easier, faster, and more accurate than any other type of input device. They are rugged, reliable, and especially well-suited for harsh or hostile environments, from the flight deck to the battlefield.

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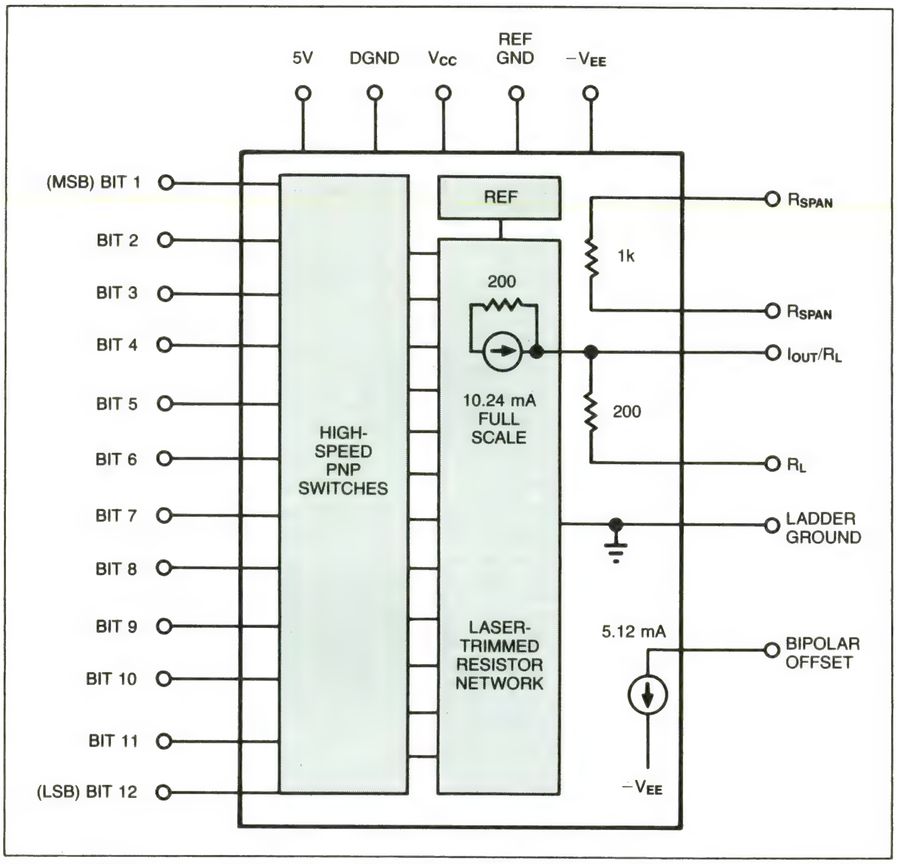
CIRCLE NO 62

D/A-converter IC uses bipolar process to provide 12-bit settling in 50 nsec



A monolithic 12-bit D/A converter that rivals more expensive hybrid units, *the AD568 current-output D/A converter is suitable for vector-scan displays and waveform generation, as well as for use in high-resolution, subranging A/D converters. A proprietary complementary bipolar process is responsible for the device's fast settling speed.*

Fabricated with a complementary bipolar process, the AD568 12-bit D/A converter offers a settling time of 50 nsec typ to within a ±0.025% error band. For its precision resistors, the current-output device uses thin films of two different resistivities. The use of the two different films, according to the manufacturer, provides for stable bit weighting and, at the same time, provides low impedance at the output, which is a necessary attribute for fast settling.

The inclusion of a buried zener reference and a bipolar-offset current source allows you to configure (by using jumpers) full-scale output-current ranges of ±5.12 mA and 0 to 10.24 mA. By using an external op amp and the on-chip span resistor, you can configure the converter for output-voltage ranges of ±5.12V and 0 to −10.24V. The compliance range of the current-output stage is typically +1.2 to −2.5V.

Responsible for the AD568's speed is the IC's complementary bipolar process, which allows the manufacturer to make both npn and pnp transistors that have gain-bandwidth products greater than 500 MHz, BV_{CEO} specs greater than 36V, and equal h_{FE} figures. In contrast, the traditional npn/pnp fabrication technique, which uses a buried-collector process, produces lateral pnp transistors that are inadequate: They have gain-bandwidth products of only about 10 MHz.

Nonlinearity specs for the AD568 comprise integral nonlinearity (straightness of the device's transfer function, drawn through end points) and monotonicity. The integral nonlinearity spec is ±0.5 and ±0.25 LSB max at 25°C for standard-and premium-grade AD568s, respectively. Over 0 to 70°C, these specs are ±0.75 and ±0.5 LSB max. The model specified for −55 to +125°C operation specs ±0.5 LSB max at 25°C and ±0.75 LSB max over temperature. All models guarantee monotonicity over the full operating-temperature range.

Other specs for the AD568 include 3-ppm/°C max unipolar offset drift and 15-ppm/°C max bipolar offset drift. Max full-scale (gain) drift is 50 ppm/°C for the standard and military-temperature models and 30 ppm/°C for the premium-grade device. Operating from ±12 or ±15V supplies, the converter draws 32 mA typ from the positive supply and 8 mA typ from the negative supply. The D/A converter's digital inputs are compatible with TTL or 5V CMOS logic families. Housed in a 24-pin, 300-mil plastic or ceramic DIP, devices in the AD568 Series start at $40 (100).—***Bill Travis***

Analog Devices Inc, 2 Technology Way, Norwood, MA 02062. Phone (617) 329-4700.

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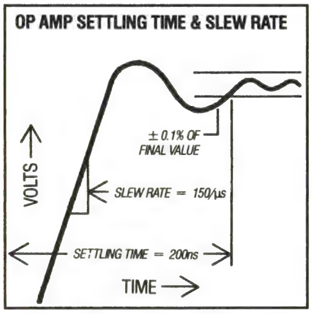
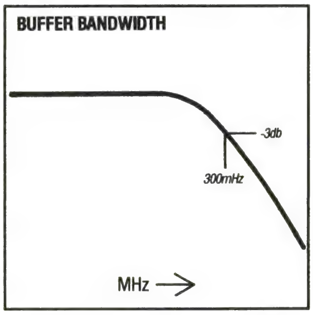
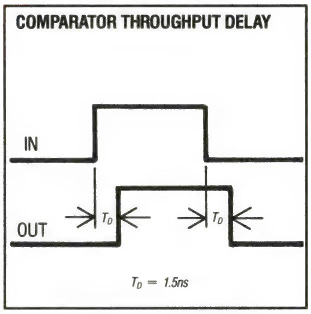
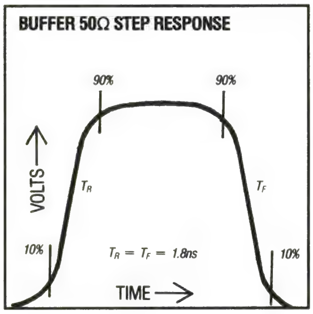

OP AMP SETTLING TIME & SLEW RATE


BUFFER BANDWIDTH


COMPARATOR THROUGHPUT DELAY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VTC's High-Performance Linear Processes	Minimum Geometry	Metal Layers	Bandwith	
			F_T NPN	F_T PNP
Complementary Bipolar Process (CBP)	2µ	2	6GHz	500MHz
ECL 2.5	2µ	2	6GHz	100MHz
Linear High-Density (LHD)	3µ	2	1GHz	100MHz

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CIRCLE NO 63

NEW!

VA033 UNITY GAIN BUFFER. Featuring high slew rate (1800 V/µs), wide bandwidth (300MHz), high output drive (±100mA), and low offset voltage (5mV).

NEW!

VC7695 ULTRA-FAST COMPARATOR. With 1.5ns delay, less than 0.5ns latch set-up time, and low input offset voltage of 5mV. Also available in a dual version (VC7697).

OTHER LSP PRODUCTS AVAILABLE NOW FROM VTC:

- **VA700 High-Speed/Precision Op Amp Family**
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  - Adjustable gain (8 to 600)
  - 100MHz bandwidth
  - Low input noise (12µV RMS)
  - No frequency compensation required
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  - Wide gain bandwidth (6MHz)
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  - High output drive (±25mA)

All products available in cerdip, PDIP, SOIC, or metal can packages, or in die form.

WATCH FOR MORE ADDITIONS TO VTC'S GROWING LINE OF LSP PRODUCTS!

CIRCLE NO 63

PC-based board and VAX link enhance 32-bit workstation

Four interface products enable you to run PC-based software on Sun workstations, interface Sun workstations to PCs and compatible computers, and make Sun workstations communicate with members of the DEC VAX family. Using these hardware and software packages, you can run applications on any of these systems and share files among all of these systems.

The Sun Integrated Personal Computer (IPC) is a coprocessor board that provides compatibility with the PC/AT. The board, which plugs into Sun workstations, lets you run MS-DOS applications in a window under the company's Unix operating system.

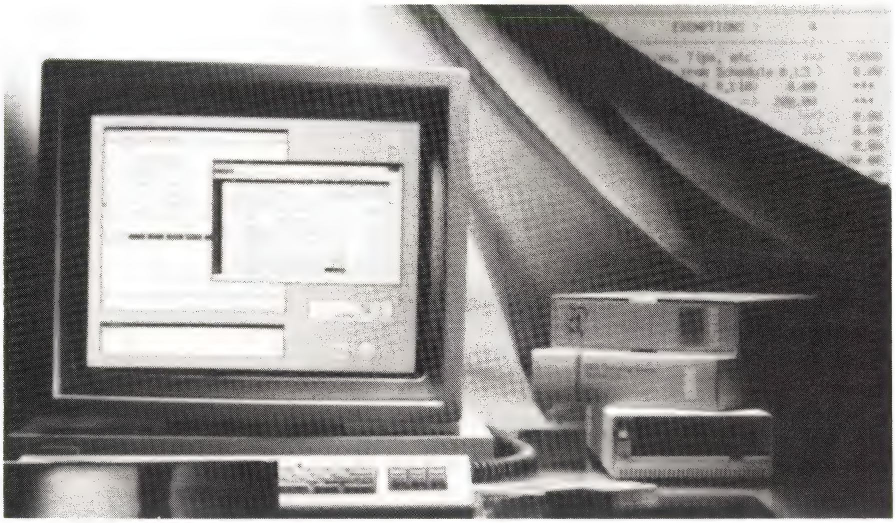
The IPC board contains a 10-MHz 80286 µP and 1M byte of memory. Because the board features an expanded-memory spec, it lets MS-DOS applications access as much as 4M bytes of memory.

The board executes color and monochrome applications; either an IBM AT color graphics adapter or a Hercules monochrome adapter can control the display. An optional 8-MHz 80287 floating-point coprocessor chip is available, as are 1.2M-byte and 360k-byte floppy-disk drives.

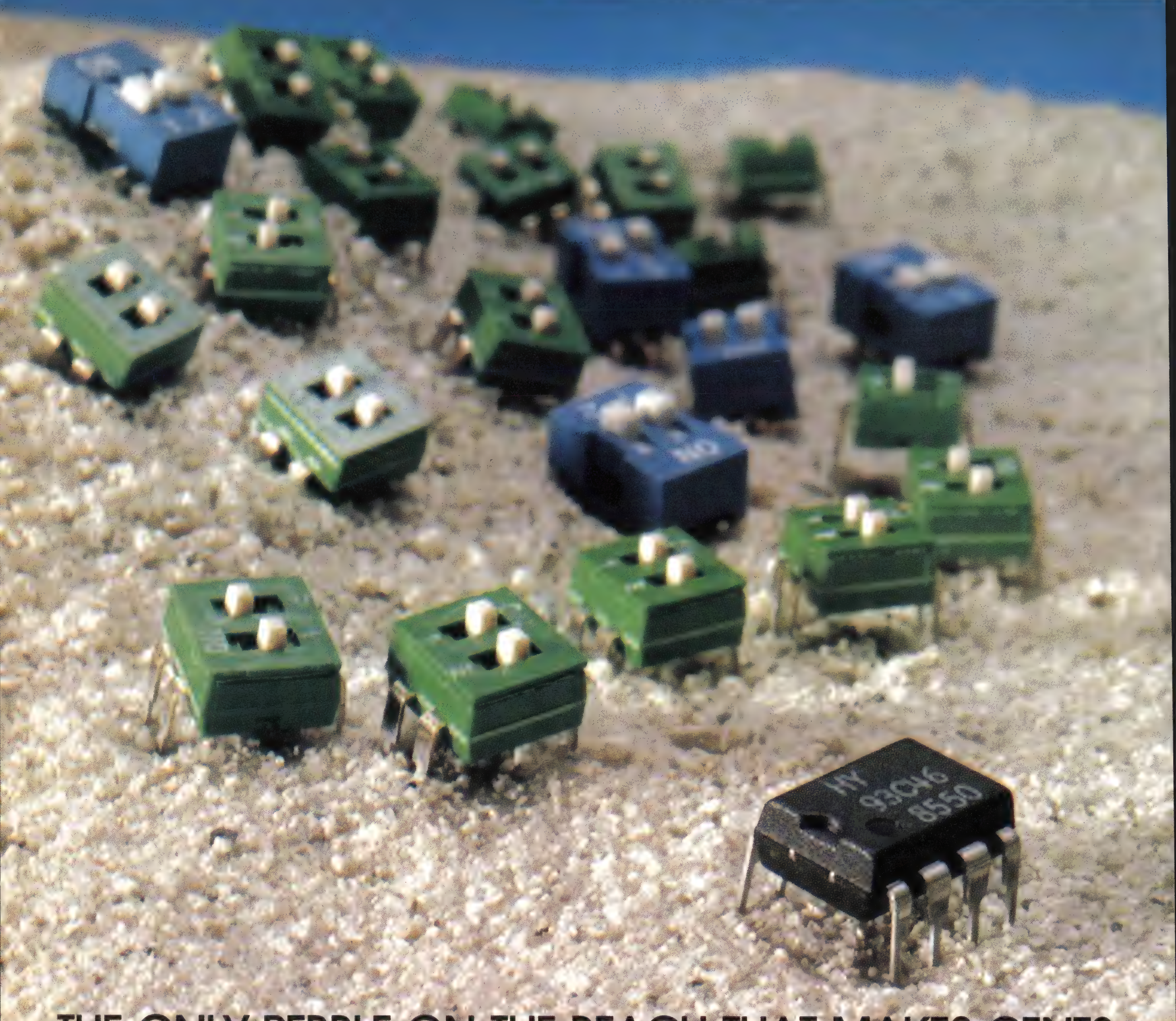
Although an IPC card must plug into a Sun workstation, several workstations can share the resources of the card via a LAN. The Sun IPC costs $1995. Accompanying software costs $395 for a single-user version; the multiple-access version is $995.

In contrast to the IPC card, which lets Sun workstations access PC capabilities, the PC-NFS program lets PCs access files in a Sun workstation. The PC-NFS software automatically converts local MS-DOS filenames to network-compatible Network File System (NFS) pathnames.

When you use PC-NFS, your network server can store data from a PC and transfer files from the PC to a 32-bit workstation. Although other members of your network can't directly access files on your PC, you can save files on a server



The 10-MHz 80286-based coprocessor board *in the Sun Integrated Personal Computer enables Sun workstations to run MS-DOS applications from within the workstations' Unix operating system.*



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Hyundai introduces a 1K EEPROM that performs the same function as several DIP switches.

The HY93C46 1K Serial EEPROM is intended for applications which require non-volatile storage of data. Our EEPROM is a 1024-bit memory organized as 64 registers of 16 bits each.

Programming for switch function is achieved by writing either a 1 or 0 in the appropriate register. Because data is written in or read out serially, no address or data bus is required–resulting in an 8-lead DIP.

Hyundai's HY93C46 is fabricated in floating-gate CMOS EEPROM technology for low power consumption, and operates on a single 5V supply. The programming voltage is generated on-chip and controlled by internal logic.

So, if you need switch setup capability, why fill your board with DIP switch components when you can use a single chip? All it takes is one HY93C46–to save component cost, reduce boards space, lower power dissipation, and improve system reliability.

The HY93C46 accommodates up to 10,000 erase/write cycles per register. Function reprogramming is easily accomplished through seven 9-bit instructions that control read, write and erase operations.

A practical alternative, the HY93C46 is available now. And Hyundai is as near as your telephone.

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WASHINGTON / OREGON, Quest Marketing Inc., (206) 747-9424; **TEXAS,** Technology Sales, (214) 437-5881

CIRCLE NO 69

and give the others transparent access to the files. The package also permits the transmission of data to a laser printer.

In quantities of 100, PC-NFS costs $225 per unit without documentation; $305 with documentation. When bundled with an Ethernet interface and documentation, the package costs $995 per unit.

By linking PC-based software to Unix-based databases, Network Innovations' Multiplex/NFS complements the capabilities of PC-NFS. Multiplex/NFS lets you read the contents of a database on a Sun workstation and transfer the data—in PC format—to a PC. The program also lets you run, on a workstation, programs that require greater computational power than a PC can provide.

You don't need to maintain a copy of Multiplex/NFS on every system in your network; you simply download the package to your PC when you use it. Site licenses of the program cost $1195.

Win/VX does for the VAX what Multiplex/NFS and PC-NFS do for the PC. The VAX-based package, from Wollongong Group, lets you access VAX and MicroVAX computers from your PC via Sun Microsystems' NFS.

Using this software, you can run an application on a VAX and transfer the output of the program to a Sun workstation. Furthermore, you can use the large storage capacity of a VAX to back up your 32-bit workstation. The VAX version of Win/VX costs $5000; the MicroVAX version is $2500.—***Eva Freeman***

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. TLX 287815.
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Network Innovations Corp, 4691 Albany Circle, San Jose, CA 95129. Phone (408) 249-6767.
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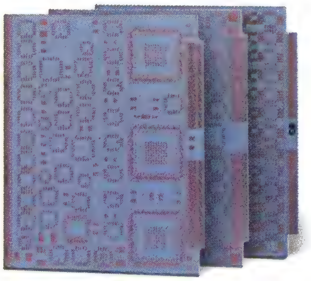

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CIRCLE NO 66

Now Hewlett-Packard users can choose...

from two new mass storage solutions from Bering Industries. The Series 8000-EP and TopSecret Removable Hard Disk Subsystems. Designed for HP computers using CS/80 and SS/80 command sets, like HP1000, HP3000, and HP9000 Series 200/300/500 systems.

Bering Series 8000-EPs and TopSecret Removable Hard Disk Subsystems are HP-IB compatible and designed for any HP computer using CS/80 and SS/80 command sets.

Enhanced Performance 8000-EP

Bering's Series 8000-EP enhanced performance hard disk subsystems offer an alternative HP mass storage solution. From 65MB to 190MB, the EPs are worth a close look.

Cost Savings. At $60 per MB, EPs are price/performance leaders. Savings can be up to 45% the cost of a comparable HP drive. And Bering's standard one-year warranty applies to all EP models.

Capability. Designed for HP users' critical performance needs in real-time and multi-user environments, the EPs are the best choice. An advanced disk controller and fast head seek mechanism match average transfer rates of HP7912/7914 drives.

Compatibility with HP-IB. The EPs are designed for any HP computer using CS/80 and SS/80 command sets. Compatibility is guaranteed. No hardware or software changes are needed for installation.

Compact. EPs save prime office or lab real estate. At one-third the size of an HP7912/7914, EPs are compact and ideal for stacking or rack mounting.

Topsecret Removables

Data Security. Securing classified data is easy with 5.25″ TopSecret removable hard disks. Sensitive information can be locked away in a safe, 10MB at a time. Personal data storage and selective file back-up is convenient and fast.

Unlimited Storage. With a TopSecret, storage is virtually unlimited simply by inserting another cartridge. No need to buy another drive to increase capacity. A two-sided built-in 3.5″ floppy is optional.

Bering has set the pace for innovative mass storage solutions in the HP world since 1981. Bering is an official HP Independent Hardware Vendor with authorized service and support by DATAGATE in the USA, and by DATATECH in Canada. For complete specifications on the EPs, the TopSecret, and 100 other disk configurations, call or write us today!

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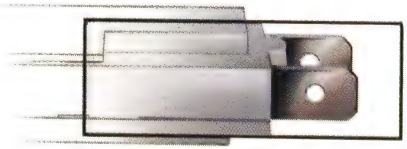
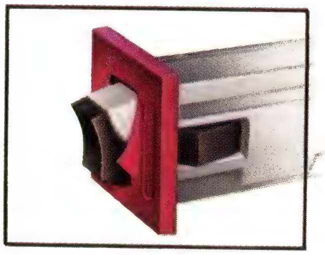
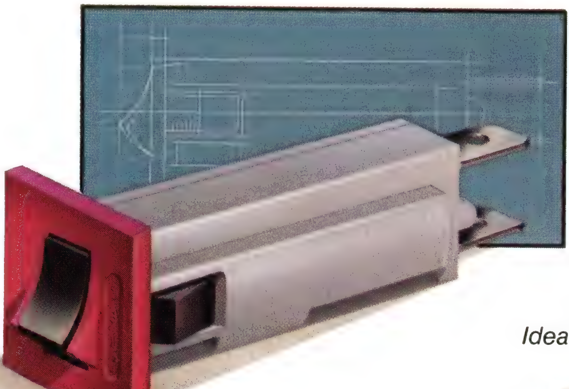


- *.250" quick-connect terminals make wiring easy.*

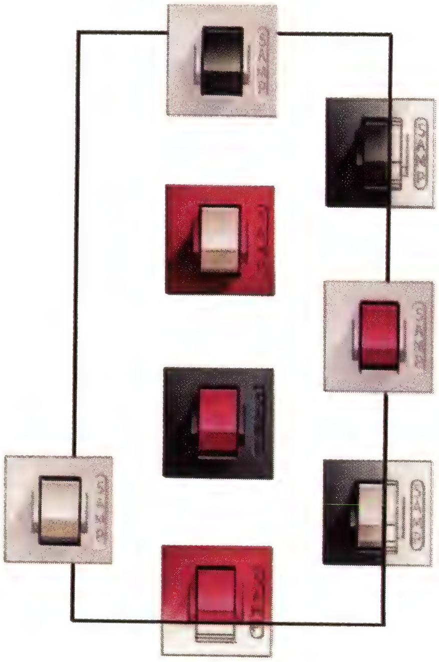
- *Trip indicator warns of a possible circuit problem. Choice of red or white.*



- *Special molded clips snap securely into standard ⅝" panel cutouts. No redesign or repunching.*



- *Variety of bezel and button colors permit color coding of circuits. Ideal for convenient up front control panel location.*



P&B's new snap-in circuit breakers end fuse replacement worries.

Our W28 series thermal circuit breakers fit the same cutout as many ⅝" fuseholders. And from 0.25 through 15 amps these UL recognized and CSA certified breakers do the same job as fuses. Only better. When the W28 trips, an indicator pops out to warn of a possible circuit problem. After the trouble is located and corrected, the W28 can be reset by simply pushing a button. But it can't be pulled out to disconnect the circuit.

Easy To Install. Wherever you presently use glass cartridge fuseholders, W28s can replace them without panel redesign or repunching. Think about putting them out front. That way they're easily accessible and their attractive appearance will add to your product's appeal. W28 breakers can be prewired and then snapped securely into the panel from the front.

Helps Sell Your Product. For everything from home entertainment equipment to medical instruments to industrial test gear, W28 breakers add selling points to your product. Good looks. The convenience of not searching for fuses. Protection against improper fuse rating substitutions. And they save the cost and trouble of maintaining a fuse inventory.

Write For Our Catalog. Find out about the economical W28 and our full line of magnetic and thermal circuit breakers. They're available off-the-shelf from authorized P&B distributors backed by our sizable factory inventory. Or contact your local P&B sales representative. Potter & Brumfield Inc., 200 South Richland Creek Drive, Princeton, Indiana 47671-0001.
Call toll free **800/255-2550.**

8609

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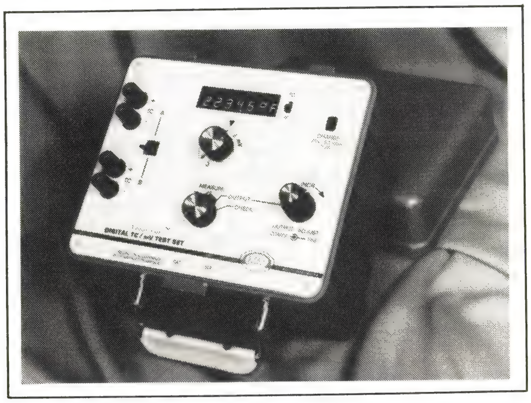
CIRCLE NO 68

READERS' CHOICE

Of all the new products covered in EDN's **June 12, 1986,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **June 12, 1986,** issue.

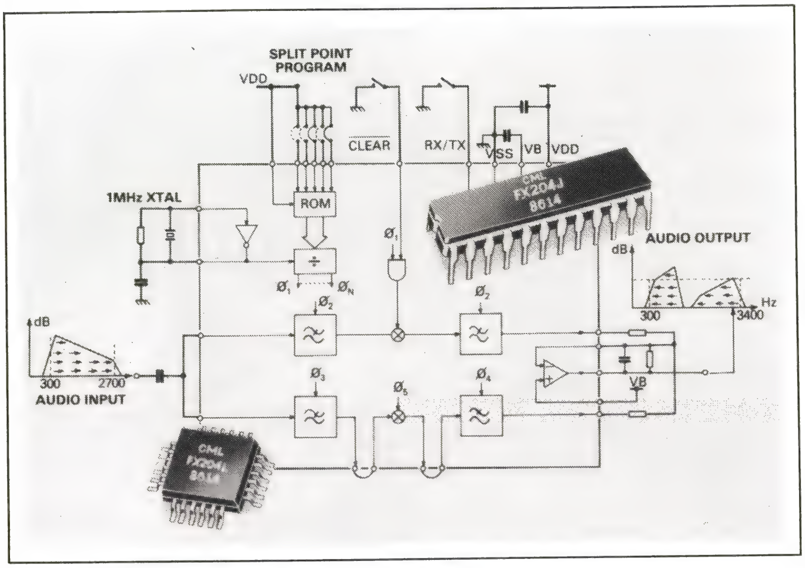
▶CALIBRATOR

The Versa-Cal has temperature sensors embedded within the binding post to maintain accurate reference-junction compensation (pg 262).
Biddle Instruments.
Circle No 604



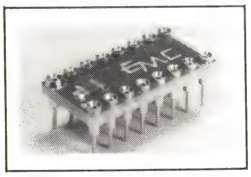
▲MEMORY CARTRIDGE

The DS1217M 1M-bit nonvolatile memory cartridge provides a simple way to plug custom applications into your general-purpose µP-based computer system (pg 101).
Dallas Semiconductor. Circle No 607



▲FREQUENCY-INVERTER IC

The FX204 performs scrambling or descrambling of speech on one chip. It splits voice band information into high- and low-frequency bands, then inverts each band around its center frequency (pg 87).
Consumer Microcircuits Ltd (European). Circle No 605
Mx-Com Inc (USA). Circle No 606

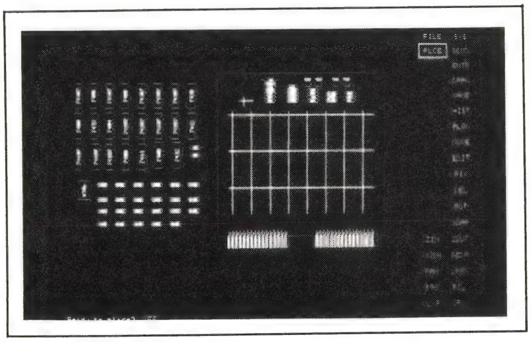


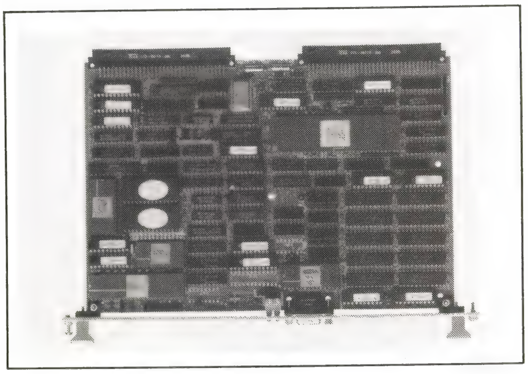
▲IC SOCKET

The Silencer combines a socket with a decoupling capacitor within the same physical area of standard sockets (pg 236).
Electronic Molding Corp. Circle No 602

▶AUTOMATIC PLACER

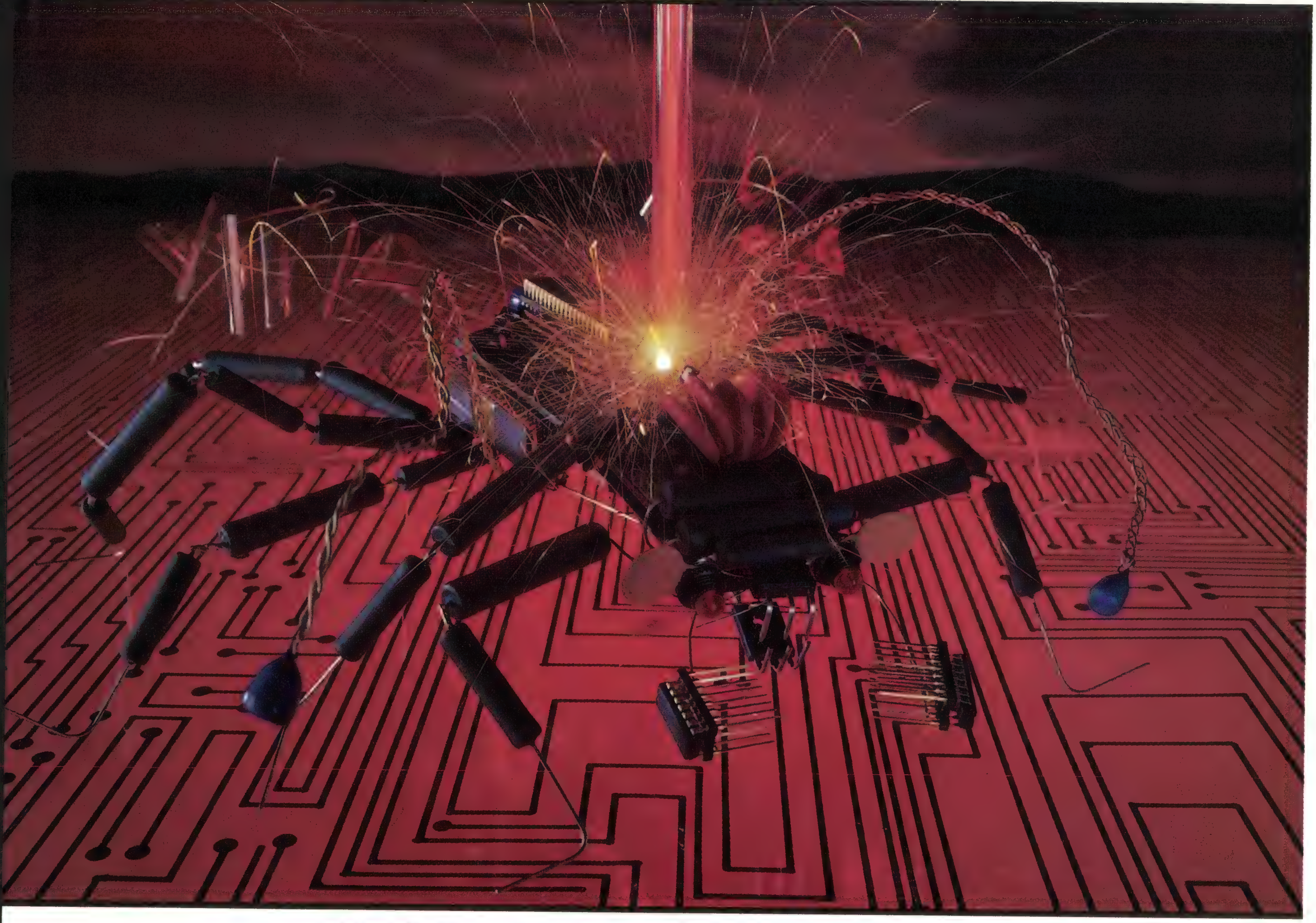
PC-Place automatically optimizes component placements for pc-board layouts (pg 220).
Personal CAD Systems Inc.
Circle No 601





▲VME LAN BOARD

The NETPC/VME LAN board uses carrier-band data transmission over the IBM Cabling System and features a 68008 CPU and a WD2840 LAN controller (pg 248).
Beal Communications. Circle No 603



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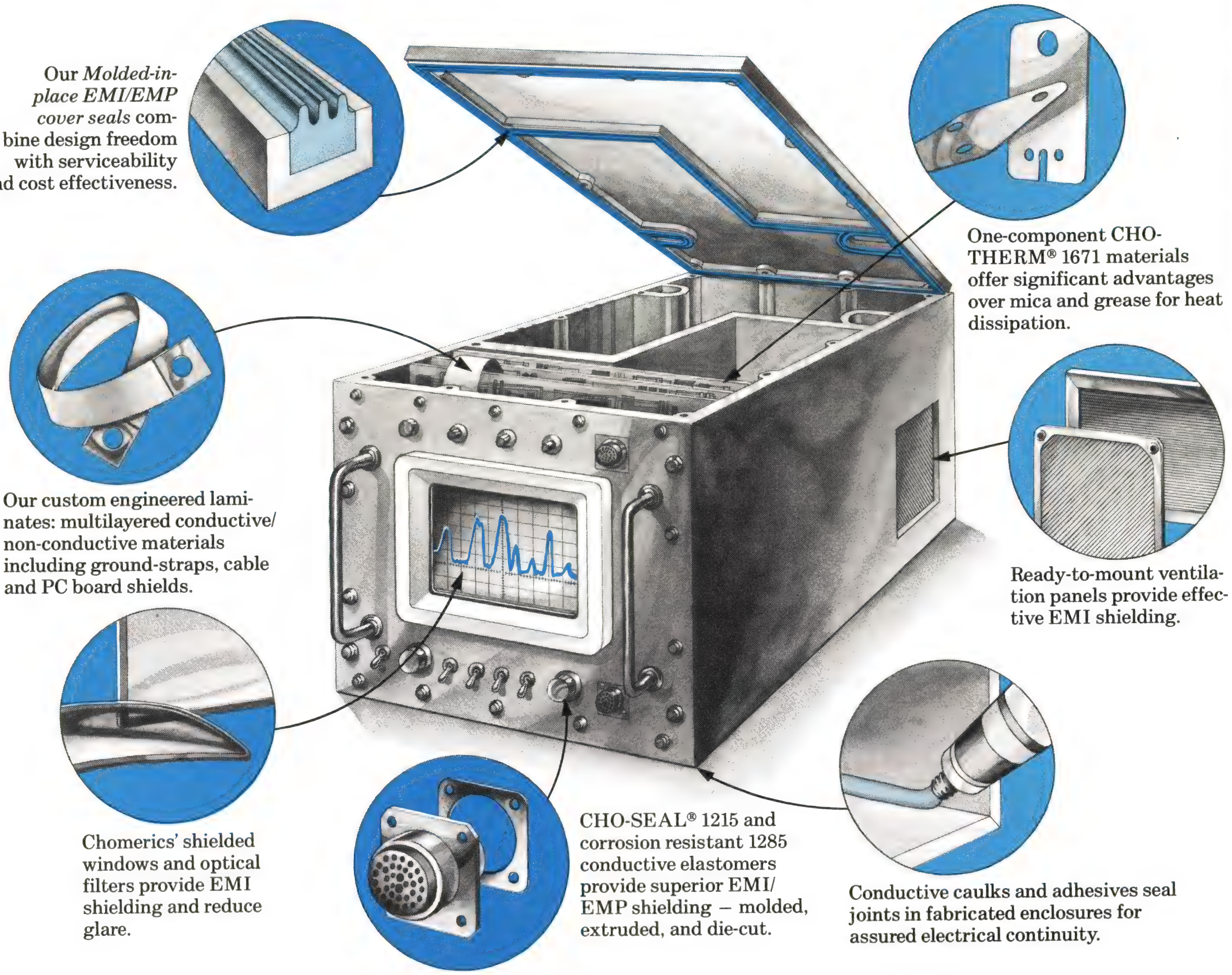
CIRCLE NO 75

TODAY'S MILITARY ELECTRONICS HAVE CHOMERICS WRITTEN ALL OVER THEM.



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CIRCLE NO 70

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MODEL	**WM100**	**MB100**	**BC100**
DIMENSIONS	1.875"x4"x7.5"	1.875"x4"x7.5"	1.875"x4"x7.5"
INPUT	320-480 Hz 115V ac ± 10%	47-65 Hz 115V ac ± 10%	dc 22-32V dc —
OUTPUT	100 watts	100 watts	100 watts
single	5,12,15,24,28V	5,12,15,24,28V	5,12,15,24,28V
triple	5 ± 12V or 5 ± 15V	5 ± 12V or 5 ± 15V	5 ± 12V 5 ± 15V
SWITCHING FREQUENCY	200 kHz	200 kHz	200 kHz
EFFICIENCY	65%-80%	65%-80%	65%-80%
RIPPLE/NOISE	0.5%-2%	0.5%-2%	0.5%-2%
LINE & LOAD REGULATION	10 mV	10 mV	10 mV
EMI	MIL-STD-461B	MIL-STD-461B	MIL-STD-461B
ENVIRONMENT	MIL-STD-810C MIL-S-901C	MIL-STD-810C MIL-S-901C	MIL-STD-810C MIL-S-901C
INPUT PROTECTION	MIL-STD-704D	MIL-STD-1399	MIL-STD-704D
TEMPERATURE			
operating	−55°C to +100°C	−20°C to +71°C	−55°C to +100°C
storage	−65°C to +125°C	−55°C to +85°C	−65°C to +125°C
MTBF* (minimum—ground benign)	99,408 hours	97,935 hours	140,000 hours

*MIL-STD-217D (50°C baseplate)

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MILITARY POWER SUPPLIES

CIRCLE NO 71

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	0	67	33	0	0	10.7	8.0
Pot-Core	0	25	50	25	0	0	8.5	10.0
Laminate (power)	20	20	50	10	0	0	6.0	8.5
CONNECTORS								
Military panel	11	0	34	22	22	11	15.4	8.0
Flat/Cable	14	43	43	0	0	0	4.3	5.0
Multipin circular	0	25	59	8	8	0	8.7	8.7
PC	0	57	43	0	0	0	4.6	6.0
RF/Coaxial	9	37	36	9	9	0	7.5	10.5
Socket	18	27	55	0	0	0	4.9	6.9
Terminal blocks	15	31	54	0	0	0	4.9	4.7
Edge card	20	20	60	0	0	0	5.2	7.4
Subminiature	0	20	40	20	20	0	12.0	6.0
Rack & panel	0	0	100	0	0	0	8.0	12.0
Power	14	29	43	14	0	0	6.3	8.4
PRINTED CIRCUIT BOARDS								
Single-sided	0	50	43	7	0	0	5.6	3.8
Double-sided	0	45	55	0	0	0	5.3	14.2
Multilayer	0	33	67	0	0	0	6.0	7.0
Prototype	0	75	17	0	0	8	5.4	2.4
RESISTORS								
Carbon film	47	20	33	0	0	0	3.1	4.3
Carbon composition	28	36	29	7	0	0	4.1	6.0
Metal film	27	20	53	0	0	0	4.7	5.1
Metal oxide	0	29	71	0	0	0	6.3	7.0
Wirewound	17	33	33	17	0	0	6.0	6.8
Potentiometers	13	20	40	27	0	0	7.9	8.4
Networks	30	30	30	10	0	0	4.6	6.4
FUSES	55	18	27	0	0	0	2.5	3.5
SWITCHES								
Pushbutton	33	25	42	0	0	0	3.8	6.3
Rotary	0	50	50	0	0	0	5.0	8:3
Rocker	10	40	40	10	0	0	5.6	8.3
Thumbwheel	0	25	75	0	0	0	6.5	8.4
Snap action	20	40	40	0	0	0	4.0	8.5
Momentary	0	25	75	0	0	0	6.5	6.0
Dual in-line	0	50	50	0	0	0	5.0	8.5
WIRE AND CABLE								
Coaxial	25	67	8	0	0	0	2.0	4.3
Flat ribbon	14	57	29	0	0	0	3.4	2.7
Multiconductor	14	57	14	15	0	0	4.6	4.5
Hookup	38	50	12	0	0	0	2.0	1.9
Wire wrap	29	43	28	0	0	0	3.1	2.9
Power cords	18	41	41	0	0	0	4.1	5.6
Other	0	0	100	0	0	0	8.0	4.8
POWER SUPPLIES								
Switching	0	0	100	0	0	0	8.0	8.4
Linear	0	57	43	0	0	0	4.6	8.3
CIRCUIT BREAKERS	10	30	60	0	0	0	5.4	8.3
HEAT SINKS	29	47	12	12	0	0	3.8	4.8

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	17	50	25	8	0	0	4.3	8.2
PC board	0	33	33	34	0	0	8.7	10.6
Dry reed	0	0	100	0	0	0	8.0	8.7
Mercury	0	0	100	0	0	0	8.0	8.7
Solid state	20	40	40	0	0	0	4.0	8.6
DISCRETE SEMICONDUCTORS								
Diode	23	24	35	12	6	0	6.7	5.9
Zener	14	29	36	21	0	0	6.9	5.9
Thyristor	0	0	40	60	0	0	12.8	7.6
Small signal transistor	0	40	30	30	0	0	8.0	6.3
FET, MOS	0	20	40	40	0	0	10.0	9.3
Power, bipolar	0	0	50	25	25	0	14.5	6.7
INTEGRATED CIRCUITS, DIGITAL								
CMOS	0	40	20	40	0	0	8.8	9.3
TTL	14	14	43	29	0	0	8.3	8.3
LS	22	11	44	22	0	0	7.3	9.5
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	0	67	33	0	0	10.7	12.0
OP amplifier	13	25	38	12	12	0	8.8	11.4
Voltage regulator	9	37	27	9	18	0	9.1	9.8
MEMORY CIRCUITS								
RAM 16k	0	0	75	25	0	0	10.0	10.3
RAM 64k	0	0	75	25	0	0	10.0	10.0
RAM 256k	0	0	67	0	33	0	14.0	8.3
ROM/PROM	0	0	67	33	0	0	10.7	11.0
EPROM	0	25	38	37	0	0	9.5	9.6
EEPROM	0	0	67	33	0	0	10.7	9.1
DISPLAYS								
Panel meters	13	25	37	25	0	0	7.5	10.0
Fluorescent	20	20	60	0	0	0	5.2	12.0
Incandescent	17	33	50	0	0	0	4.7	8.7
LED	0	36	55	9	0	0	6.5	6.9
Liquid crystal	0	25	63	12	0	0	7.5	9.7
MICROPROCESSOR ICs								
8-bit	0	25	50	25	0	0	8.5	10.3
16-bit	0	20	60	0	0	0	10.4	7.1
FUNCTION PACKAGES								
Amplifier	0	0	50	50	0	0	12.0	10.7
Converter, analog to digital	0	25	50	25	0	0	8.5	10.6
Converter, digital to analog	0	33	33	34	0	0	8.7	11.0
LINE FILTERS	0	75	25	0	0	0	3.5	5.6
CAPACITORS								
Ceramic	8	38	46	8	0	0	5.7	6.0
Ceramic monolithic	0	25	63	12	0	0	7.5	6.4
Ceramic disc	0	55	27	18	0	0	6.2	5.8
Film	17	42	33	8	0	0	4.8	6.4
Electrolytic	14	29	43	14	0	0	6.3	6.5
Tantalum	8	31	46	15	0	0	6.8	7.1
INDUCTORS	0	33	33	34	0	0	8.7	6.0

Source: *Electronics Purchasing* magazine's survey of buyers

SIEMENS

A jump ahead in quality. Longterm failure rate 2 fit. Siemens of course.

To be ahead in electronic components you need to have your nose in front when it comes to product quality. Testing at extremes of heat and cold helps guarantee it. And a major criterion in judging quality is longterm failure rate, like the 2 fit that Siemens achieves with its capacitors.

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Not only product quality has to be right, the quality of service must be on the mark too. Dependability in delivery and on deadlines, flexibility, comprehensive documentation are just as important when you're a Siemens customer. Example: in the assessment of big customers Siemens regularly comes away with a rating of 100% on serviceability, which often means satisfying more than ten different criteria.

Siemens controls the reliability of its components through periodic environmental and longterm tests.

Example: each capacitor is tested 100% to specification.

Component quality also means using the experience fed back from applications. And here Siemens can draw from the know-how of its system experience.

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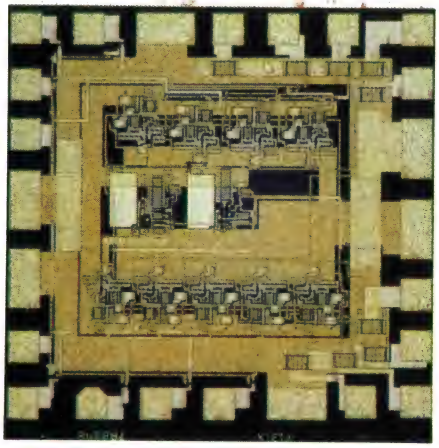
12/Z009e

High-speed glue logic plays an obvious role in a world of ever-increasing computing power, and GaAs, ECL, and CMOS remain the dominant technologies for these high-speed logic ICs. Each can claim niches in which their respective advantages prove best, but process developments will continue to create areas of competition.

High-speed logic ICs

Denny Cormier, Regional Editor

Commercial high-speed datacomm, telecomm, and supercomputer applications and such military projects as the VHSIC (very high speed ICs) project and various Defense Advanced Research Projects Agency (DARPA) programs continue to push clock rates for digital-IC interfaces well beyond the 100-MHz level. Today's glue-logic ICs must link ultrafast memories and fiber-optic I/O ports with the latest µPs for reduced-instruction-set computers (RISCs), whose speeds reach 100 MIPS and beyond. In this high-speed realm, gallium-arsenide (GaAs), ECL, and CMOS vie for some niches and stand by themselves in others.



This member of the F100K ECL IC family *from Fairchild, the F100121 9-bit inverter, drives an 8-bit, 50Ω data bus, plus parity bit, with a maximum propagation delay of only 1.6 nsec.*

The applications niches of each technology conform roughly to different speed ranges (though other factors are also important in your choice of logic ICs). Rad-hardened GaAs MSI-logic ICs clock at frequencies of 1 GHz to more than 5 GHz at high temperatures. (Devices made with enhancement-depletion technology tend to be faster than those fabricated with the older depletion-mode technology.) High-performance standard and programmable ECL bipolar chips provide an economical alternative to GaAs ICs when the desired clock speeds approach 1 GHz. Meanwhile, the latest submicron CMOS logic ICs deliver clock rates of 100 MHz and higher.

Although they remain expensive, GaAs logic ICs still give you the best performance in designs using SSI- and MSI-logic state functions at clock rates above 1 GHz. GaAs logic ICs also provide the added benefit of unsurpassed radiation hardness. The ability of GaAs substrates to absorb radiation in amounts as high as 10^7 rads (GaAs) and to withstand radiation fluxes greater than 10^{11} rads (GaAs)/sec without damage makes GaAs logic ICs ideal for many space and military applications. For optically coupled logic, GaAs ICs are the only devices that provide chip-level, solid-state laser interfaces working above 1 GHz.

You can obtain a variety of off-the-shelf GaAs parts from GigaBit Logic, Harris Microwave Semiconductor, and TriQuint Semiconductor (a Tektronix subsidiary). In March, TriQuint introduced its ECL-compatible Q-Logic Series of depletion-mode GaAs MSI glue-logic ICs. The fastest member of this family is the TQ1111-30 2-stage ripple counter, which clocks data at 3 GHz and dissipates 1.6W. The company supplies the part in a 10-pin metal-ceramic flat pack at a cost of $199 (100). TriQuint also supplies a $275 prototype evaluation kit for testing the Q-Logic parts.

A similar line of depletion-mode GaAs MSI devices, the 10G PicoLogic family from GigaBit Logic, also provides ECL compatibility. For example, the company's 10G065-2 7-stage ripple counter toggles data at a 3-GHz clock rate and typically dissipates 1.5W. The $174 (100) part comes in a 36-pin flat pack or LCC. Clocking at a 2.7-GHz rate, the 10G021A-2 dual precision D flip-flop dissipates 1.1W and provides sampling jitter of less than 1%, as well as individual clock, preset, and clear inputs. This device costs $78 (100), whether you purchase the flat pack or the LCC version.

Other GaAs logic parts recently introduced by Giga-

No matter what processing speed your application demands, *you can find high-speed glue-logic ICs—CMOS as well as ECL and GaAs—that are equal to the task. (Photo courtesy Integrated Device Technology)*

SPECIAL REPORT

MILITARY ELECTRONICS

For optically coupled logic, GaAs ICs are the only devices that provide you with chip-level solid-state laser interfaces working above 1 GHz.

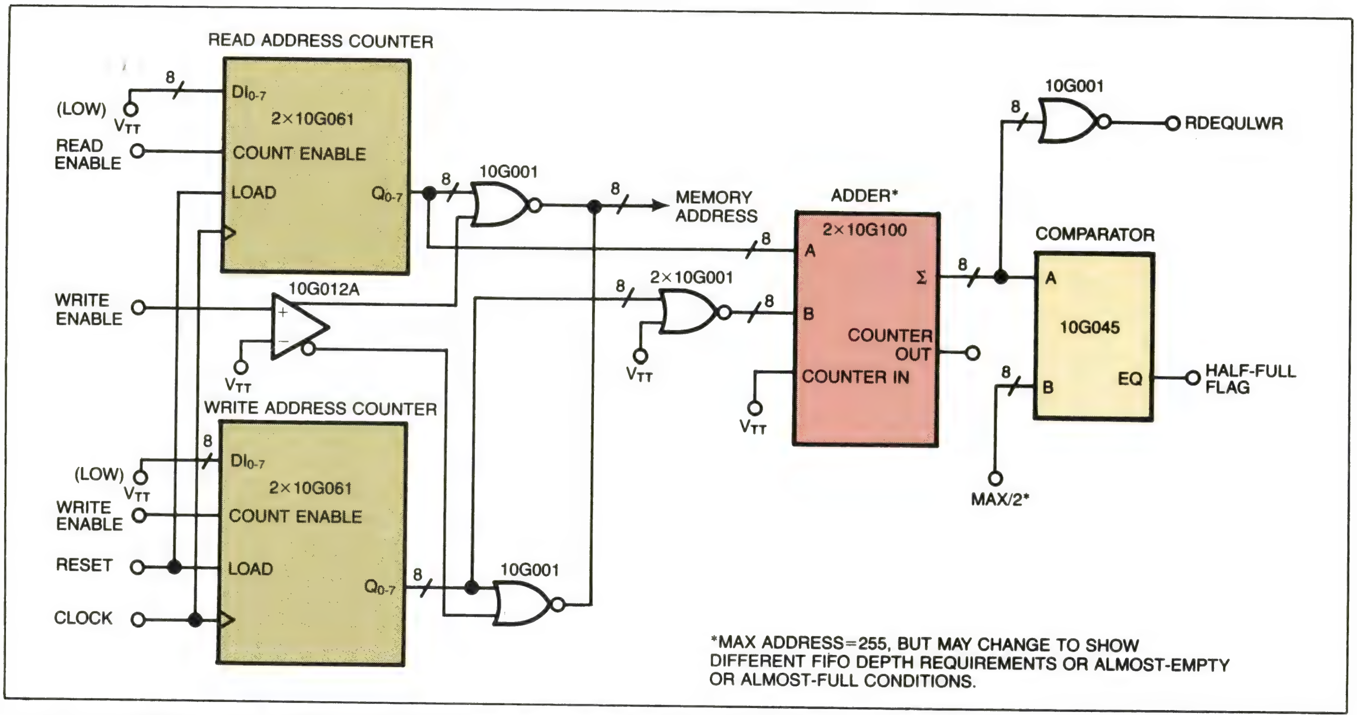
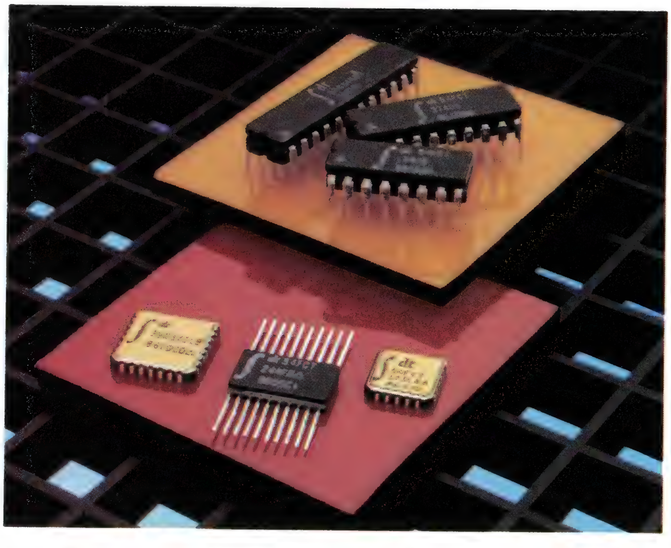


Fig 1—By combining four 10G061 carry look-ahead generators *(serving here as address counters), five 10G001 gates, a 10G100 adder, and a 10G045 comparator from GigaBit Logic's PicoLogic Series of GaAs MSI parts, you can design a FIFO controller to work with the company's 3-nsec, 256×4-bit GaAs static RAM.*

Bit include the 10G002 quad 2-input exclusive-OR gate (in a 36-pin LCC), which costs approximately $60 (100), and the 10G044 dual 2:4 decoder, priced at $85 (100) in a 40-pin LCC. Both parts spec a 600-psec propagation delay. Fig 1 shows how you can use 10G Series devices to create a FIFO controller that works with the company's 12G014 3-nsec, 256×4-bit, pipelined static RAM.

GigaBit supplies a completely assembled prototype test bed, the 10GEVAL, for $6000. The assembly includes a power supply and ECL interface circuitry. The company also provides an evaluation module in kit form, the $750 10GPDK, which handles as many as eight GaAs MSI-logic ICs.

GigaBit Logic also makes higher-density GaAs logic ICs, such as the 10G040 8:1 time-division multiplexer and 10G041 1:8 time-division demultiplexer. Both parts were introduced in April. This mux/demux chip set works especially well in designs employing fiber-optic communications circuits that clock at 750 MHz. Its $50 (1000) price tag makes the chip set comparable in price with functionally similar ECL mux/demux ICs.



Operating at clock speeds above 100 MHz, *Integrated Device Technology's IDT39C800 high-speed CMOS logic ICs can drive TTL interfaces and yet dissipate less than 10 mW. Military versions of these devices meet MIL-STD-883 Class B standards.*

As GaAs production technology continues to mature, you can expect significant reductions in prices, especially for less complex parts. Stewart Sando, GigaBit's product manager, cites improved wafer yields as the primary reason for cost reductions. The company has already achieved wafer yields comparable to those normally associated with silicon processing (70% to 80%) for such parts as the 10G000A quad 3-input NOR

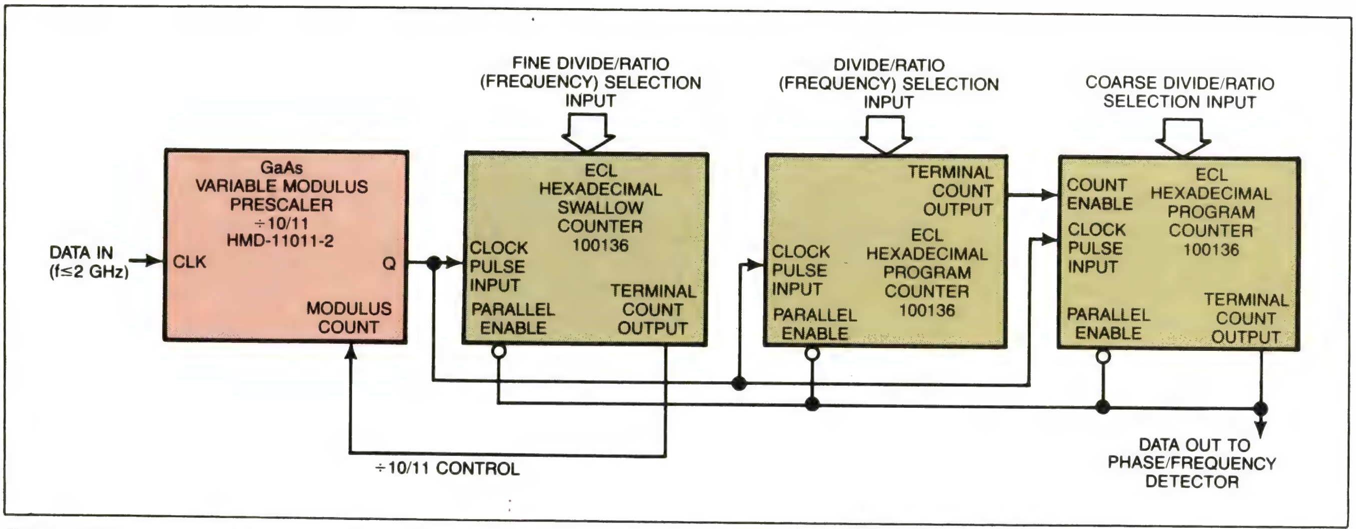
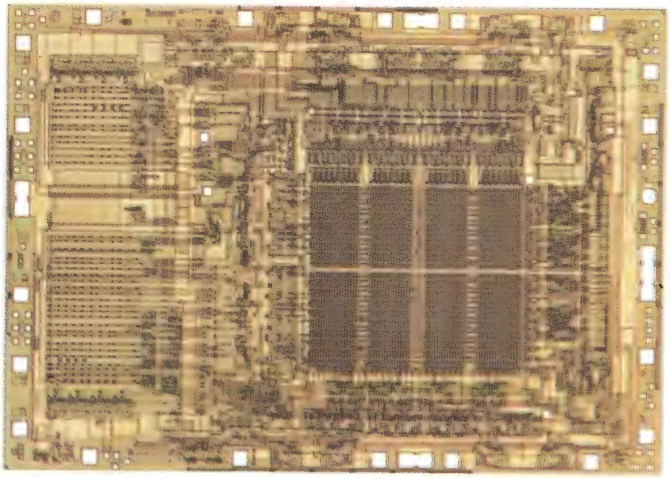

FINE DIVIDE/RATIO (FREQUENCY) SELECTION INPUT
DIVIDE/RATIO (FREQUENCY) SELECTION INPUT
COARSE DIVIDE/RATIO SELECTION INPUT
GaAs VARIABLE MODULUS PRESCALER ÷10/11 HMD-11011-2
CLK
Q
MODULUS COUNT
DATA IN (f≤2 GHz)
ECL HEXADECIMAL SWALLOW COUNTER 100136
CLOCK PULSE INPUT
PARALLEL ENABLE
TERMINAL COUNT OUTPUT
TERMINAL COUNT OUTPUT
ECL HEXADECIMAL PROGRAM COUNTER 100136
CLOCK PULSE INPUT
PARALLEL ENABLE
COUNT ENABLE
ECL HEXADECIMAL PROGRAM COUNTER 100136
CLOCK PULSE INPUT
PARALLEL ENABLE
TERMINAL COUNT OUTPUT
÷10/11 CONTROL
DATA OUT TO PHASE/FREQUENCY DETECTOR

Fig 2—You can make a pulse-swallowing programmable counter, *operating at a 2-GHz clock rate, with the HMD-11011-2 GaAs variable modulus prescaler from Harris Microwave Semiconductor. The device's ECL-compatibility allows you to connect it directly to Fairchild's F100136 ECL 4-bit counter/shift registers.*



Offered in MECL-10KH- and F100K-compatible versions, *the PL1016P8/10016P8 ECL ICs from National Semiconductor let you control eight different MSI state functions with a maximum propagation delay of 6 nsec over the full military temperature range.*

gate (290-psec propagation delay), resulting in a price of only $37.40 (100). Yields for more complex PicoLogic parts are still in the area of 60% to 70%. Nevertheless, Sando states the company has targeted wafer yields of 90% for MSI parts and more than 50% for its LSI parts within a year's time. These higher yields will translate into cost reductions of at least 30%.

Because of difficulties associated with testing, GigaBit does not, at present, guarantee its PicoLogic parts over the full military temperature range. Instead, the company's GaAs glue-logic parts operate over the 0 to 85°C range. GigaBit plans to have the PicoLogic family operating over the full military temperature range by the end of 1987.

For applications requiring at least 1-GHz operation and ECL compatibility over the full military temperature range, you can use chips from Harris Microwave's line of GaAs glue-logic ICs. For example, the company's HMD-11113-2 dual 2-input exclusive-OR gate provides a fanout of three into a 50Ω terminated transmission line. Propagation delay is 650 psec. This chip comes in a 16-pin flat pack and costs $224 (100). You can test this device in a prototype circuit when you purchase Harris's $350 HMK-11SSI-2 evaluation kit.

For such applications as programmable pulse-swallowing counters, fixed prescalers, and high-speed video processing in satellite or microwave communications equipment, you can use Harris's HMD-11011-2 GaAs signal-processing component, released in March. This chip works at 2-GHz clock rates and lets you divide an input signal by a factor of 10 or 11 **(Fig 2)**. The device, supplied in a 16-pin flat pack, costs $241 (100) and works well with Fairchild's F100K ECL parts.

Although the speeds GaAs MSI-logic parts can attain are impressive, GaAs parts tend to slow down at LSI densities. Newly introduced GaAs 2901 bit-slice μPs from Vitesse Electronics Corp (Camarillo, CA), for instance, will only clock at approximately 100 MHz. To circumvent this limitation and attain higher system speeds, supercomputer designers at Cray Research (Chippewa Falls, WI) will utilize MSI rather than LSI GaAs logic to create the CPU for its next-generation supercomputer, the Cray 3, which is already under

You can expect prices for GaAs logic ICs to fall as processing techniques improve.

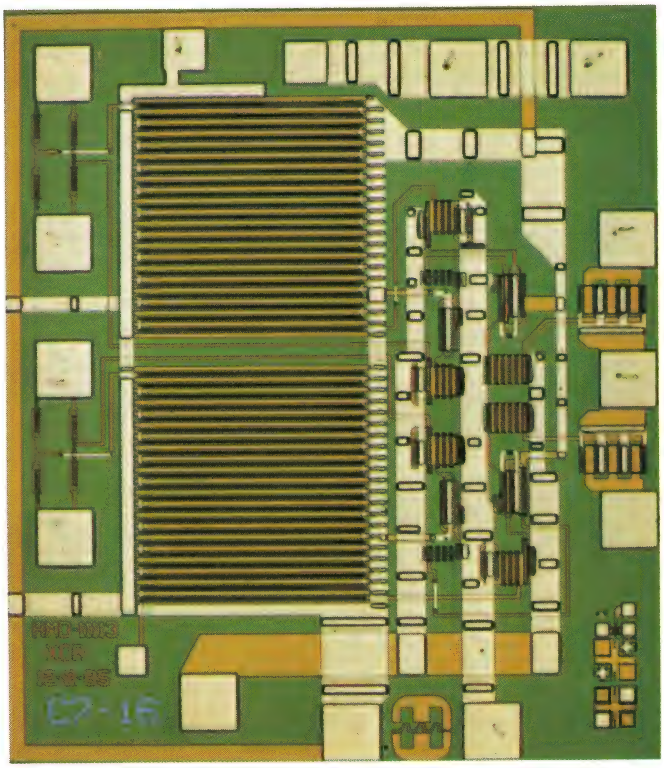
development. In addition, Cray engineers believe that GaAs MSI parts are still more reliable, offer more design flexibility at the board level, and are more readily available than current LSI ICs made with GaAs.

Even so, several companies have decided to manufacture LSI GaAs logic and memory chips, made with a more advanced enhancement-depletion process. These advanced GaAs logic chips will run at clock rates of 5 GHz and higher. One memory IC that will demand such performance from logic chips is Rockwell International's (Newbury Park, CA) GaAs, 4k-bit static RAM (made with enhancement-depletion MESFETs), which specs an access time of 5 nsec. A 16k-bit static RAM is scheduled for sampling later this year; it's intended for use in the DoD's navigational global-positioning system. Another high-speed memory is Vitesse's 3.5-nsec, 4k-bit static RAM built with enhancement-depletion GaAs transistors and scheduled for introduction later this year.

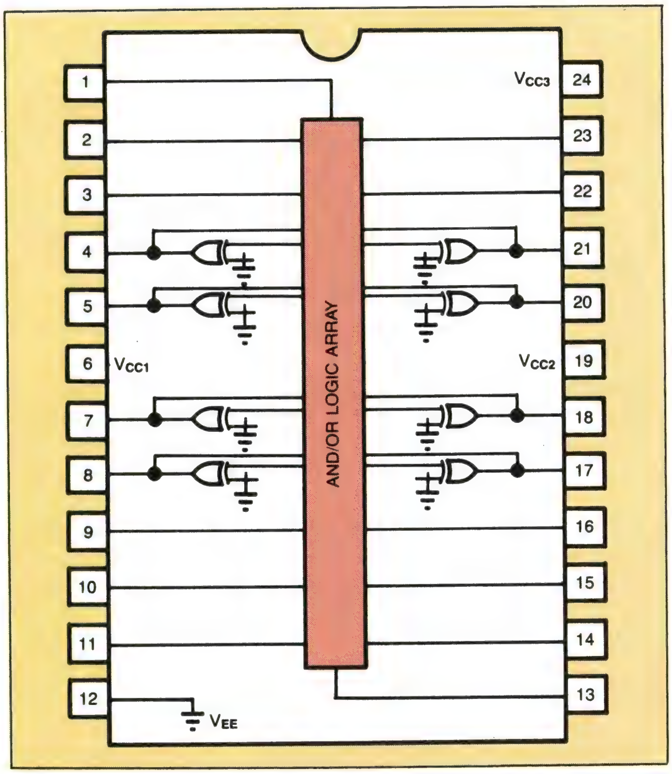
Meanwhile, other companies are making plans to manufacture complex GaAs logic devices for high-speed military and specialized industrial applications. In June, Texas Instruments announced its plans not only to produce enhancement-depletion GaAs static RAMs with an associated 200-MIPS RISC μP, but also to make GaAs logic ICs using a complex heterojunction (HIIL) process that will produce 1-GHz VLSI devices. To maintain gigahertz clock speeds at LSI densities, Honeywell has been developing a CMOS-GaAs process. In addition, the company is working on a GaAs logic IC containing a wafer-level solid-state laser for use with fiber-optic interfaces.

ECL clock speeds, densities climbing

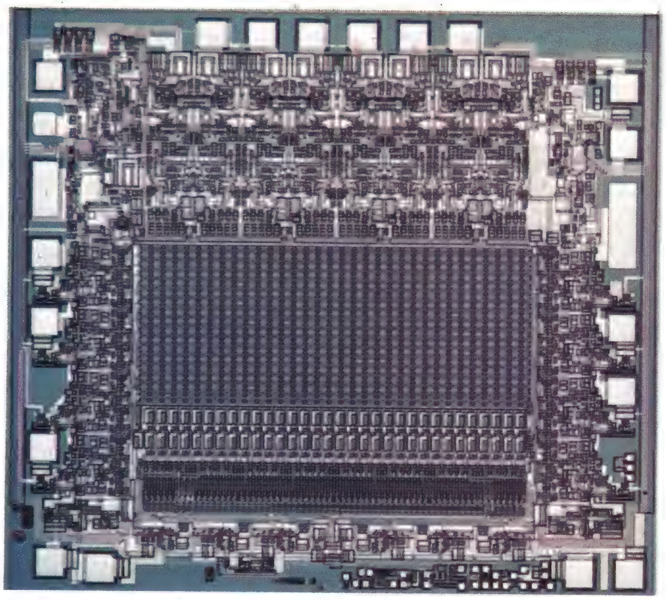
Although they require more power, ECL ICs now rival the performance of depletion-mode GaAs chips in the 1-GHz region of operation. Commercial and industrial supercomputers, superminicomputers, and engineering workstations whose performance levels exceed the capabilities of a VAX-11/780 or MicroVAX form a natural niche for ECL designs. Because they can achieve greater densities than GaAs ICs and greater speeds than CMOS parts, ECL chips are rapidly



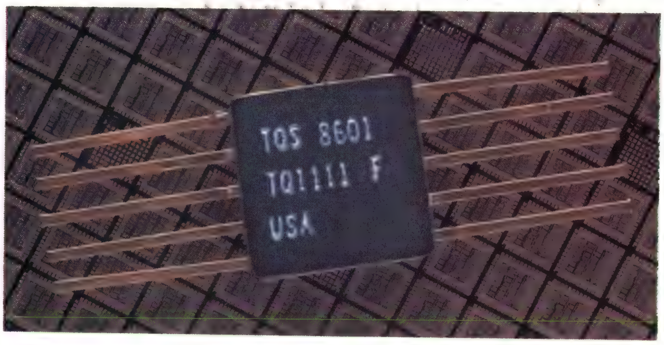
Designed specifically for radar signal processing, *parity checking, digital frequency measurement, and fiber-optic interfacing, the HMD-11113-2 GaAs dual 2-input exclusive-OR gate from Harris Microwave Semiconductor furnishes a fanout of three into 50Ω.*



This 24-pin ECL programmable logic chip, *the 6-nsec PAL10H20P8 from Monolithic Memories, gives you 12 dedicated inputs and eight outputs (with feedback) that interface directly to Motorola's MECL-10KH ECL MSI-logic ICs.*



Using internal ECL circuitry, each member of Monolithic Memories' 20-pin PAL20D Series drives eight high-speed TTL interfaces with a maximum I/O delay of 8 nsec.



***The fastest member of the Q-Logic Series of GaAs logic ICs** from TriQuint is the TQ1111-30 2-stage ripple counter, which clocks at rates as high as 3 GHz. It serves in such applications as fiber-optic communications, high-speed computer interfaces, and test instrumentation.*

emerging as the most cost-effective hardware interfaces in high-speed designs incorporating 20- to 40-MIPS μPs.

In fact, Peyton Cole, director of Fairchild's bipolar division, believes that ECL, and not GaAs technology, will dominate logic ICs used in supercomputer circuit designs for at least the next five years. To emphasize his point, Cole cites the fact that both Sierra and Gould-SEL use ECL circuitry in mainframe computers.

ECL compares favorably with GaAs and CMOS in this niche for several reasons. Performance in high-speed computer circuitry is governed not only by the gate speed within the logic ICs, but also by interconnect delays. And unless you increase circuit density, you can't attack those interconnect delays. Gate speed does become a more important factor in overall performance as densities increase, and GaAs circuits do have subnanosecond gate delays, but potential GaAs densities are still very low compared with those of ECL or CMOS circuitry.

GaAs also lacks sufficient drive capability to handle long transmission lines. Other difficulties with GaAs include lack of power-supply voltage standardization, the lack of second sources, wafer crystal defects, crosstalk problems traceable to high slew rates (>5V/nsec), and prices that remain comparatively high.

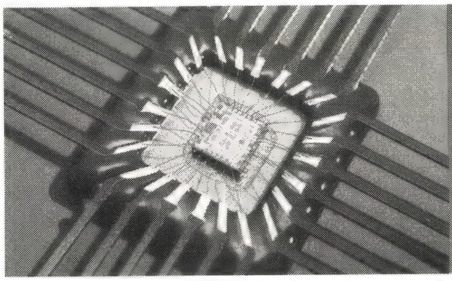
ECL's other potential competitor, CMOS, is hard to handle at high speeds, not only because of its low output-drive capability (in most cases), but also because its 5V output swings create high-frequency noise transients that contribute to interchip and intrachip crosstalk. In contrast, ECL circuitry internally switches only 800 mV.

You must deal with two aspects of the noise problem when working with high-speed logic ICs: noise generation and noise susceptibility. Sources both internal and external to the chip generate electrical noise. Crosstalk is another form of generated noise. Not surprisingly, noise components from these sources are characteristically very high in frequency, because they are principally transmitted through power sources and buses. In addition to limiting the noise generated by your logic ICs and other sources, you must ensure that the chips are not susceptible, to the point of degrading system performance, to noise that you can't eliminate.

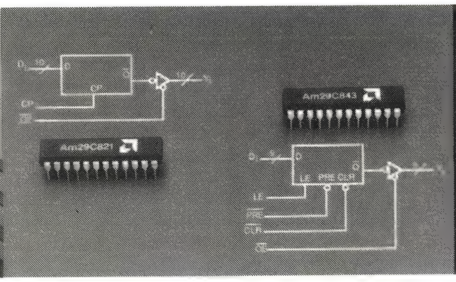
ECL chips perform well in noisy environments. Because their internal transistors are configured in a differential fashion, ECL circuits propagate less noise, and are less susceptible to noise, than their CMOS or GaAs counterparts. Furthermore, in military and space applications, logic ICs may encounter additional noise in the form of radiation. Because of their relatively high junction currents, ECL ICs are generally unaffected by neutron bombardment, even after absorbing radiation doses between 10^6 and 10^7 rads (Si).

It's for these reasons that Fairchild prefers to use ECL technology in its high-speed glue-logic chips. ECL process technologies have also been able to capitalize on breakthroughs in CMOS fabrication, because both technologies employ similar photolithographic techniques (see "High-speed digital ICs," EDN, August 22, 1985, pg 110). The company employed such fabrication technologies in the development of its F100K Series ECL

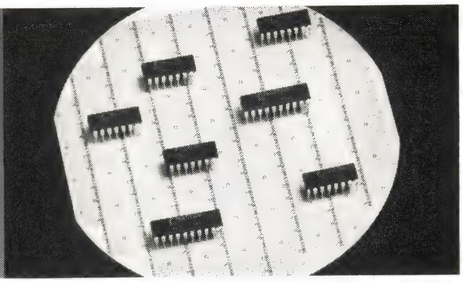
Although the speeds GaAs MSI-logic parts can attain are impressive, GaAs parts tend to slow down at LSI densities.



The FGE0050 ECL 100-gate logic array *from Fairchild helps cut interconnect delays and perform special F100K logic functions on a single chip for operation at clock frequencies as high as 600 MHz.*



These two CMOS latch/register bus interface ICs, *the Am29C821 and Am29C843 from Advanced Micro Devices, cut data-bus-interface propagation delays to 12 nsec and 11 nsec, respectively, while driving 24-mA circuits.*



A typical propagation delay of 5 nsec *is a distinctive feature of seven new members of Fairchild's 54/74/AC/ACT Fact family of high-speed CMOS logic ICs. These parts include the 74AC157/158 quad 2-input multiplexers and the 74ACT374 octal D flip-flop.*

devices. For similar reasons, Motorola has developed an extensive line of ECL devices, the MECL-10KH logic family. The company's proprietary Mosaic (Motorola oxide self-aligned implanted circuits) process keeps MECL-10KH gate delays below 2 nsec.

Propagation delay as low as 1 nsec

You will find alternatives to Motorola's MECL-10KH family from Fairchild, Hitachi, Monolithic Memories, and Signetics. MMI's MC10H101 quad OR/NOR gate is one of the fastest ECL glue-logic ICs, with a typical propagation delay of 1 nsec. Pricing for the MC10H101 is representative of this class of product: $1.26 in plastic DIPs and $1.51 in ceramic DIPs (1000).

Fairchild uses E-beam lithography to produce its higher-density ECL parts, such as its FGE0050 100-gate array, which holds gate delays to 225 psec. This particular device uses the same technology as the F100K parts and dissipates only 0.5W at 600 MHz. Honeywell supplies functionally similar, rad-hardened ECL gate arrays that work over the full military temperature range.

These improvements in manufacturing have resulted in developmental ECL chips that attain VLSI densities as high as 1,000,000 gates and speeds 10 times those of CMOS parts. Operation of these parts requires an air-cooled environment, however, because the average power dissipation for Fairchild's ECL ICs is still just less than 1 mW per gate.

In another development, low-density ECL gate arrays have made significant advances toward reducing interconnect delays at I/O interfaces. High-speed ECL devices are still the most economical means for driving memory devices that have less than 25-nsec access times.

Another practical way to cut interconnect delays is by bringing more logic on chip, which is made easier through the use of ECL programmable-array-logic devices. Monolithic Memories, Advanced Micro Devices, and National Semiconductor have all recently introduced 24-pin ECL PAL devices with 6-nsec gate delays. National's ECL PAL, the PL1016P8, costs $19.85 (100) and is compatible with Motorola's 10KH ECL devices.

Even Fairchild's Fast LSI logic ICs and Fast PLAs (programmable logic arrays) utilize internal ECL circuitry. In particular, members of the 16RPXX Fast-PLA Series feature 15-nsec gate delays with full MIL-STD-883C qualification. These devices come in 20-pin flat packs, DIPs, or LCCs, at a cost of $5.49 (100).

Reports of the diminishing applicability of ECL, and of bipolar technology generally, appear to be premature. Earlier this year, for example, TI had abandoned many of the parts made with its TTL-Impact bipolar process in favor of its 1-μm Epic CMOS process. Some of the reasons the company gave for not going to ECL included insufficient logic density (compared with CMOS), incomplete product lines, inadequate CAE design tools, difficulties in managing system cooling, and overly complex packaging. In June, however, TI apparently reassessed the technology and announced its intention to fabricate a 50-MIPS ECL version of its 74AS888 bit-slice μP using the company's Impact-X ECL process.

Fairchild's Cole believes that ECL technology, when used in conjunction with BiMOS technologies, can provide Cray 1-level performance in a desktop supermini to increase the drive capacity of CMOS LSI devices such as Fairchild's Fact family of logic ICs. Indeed, you may find that you must use ECL in conjunction with CMOS and TTL technologies in many cases—most notably in designs involving special-purpose RISC μPs

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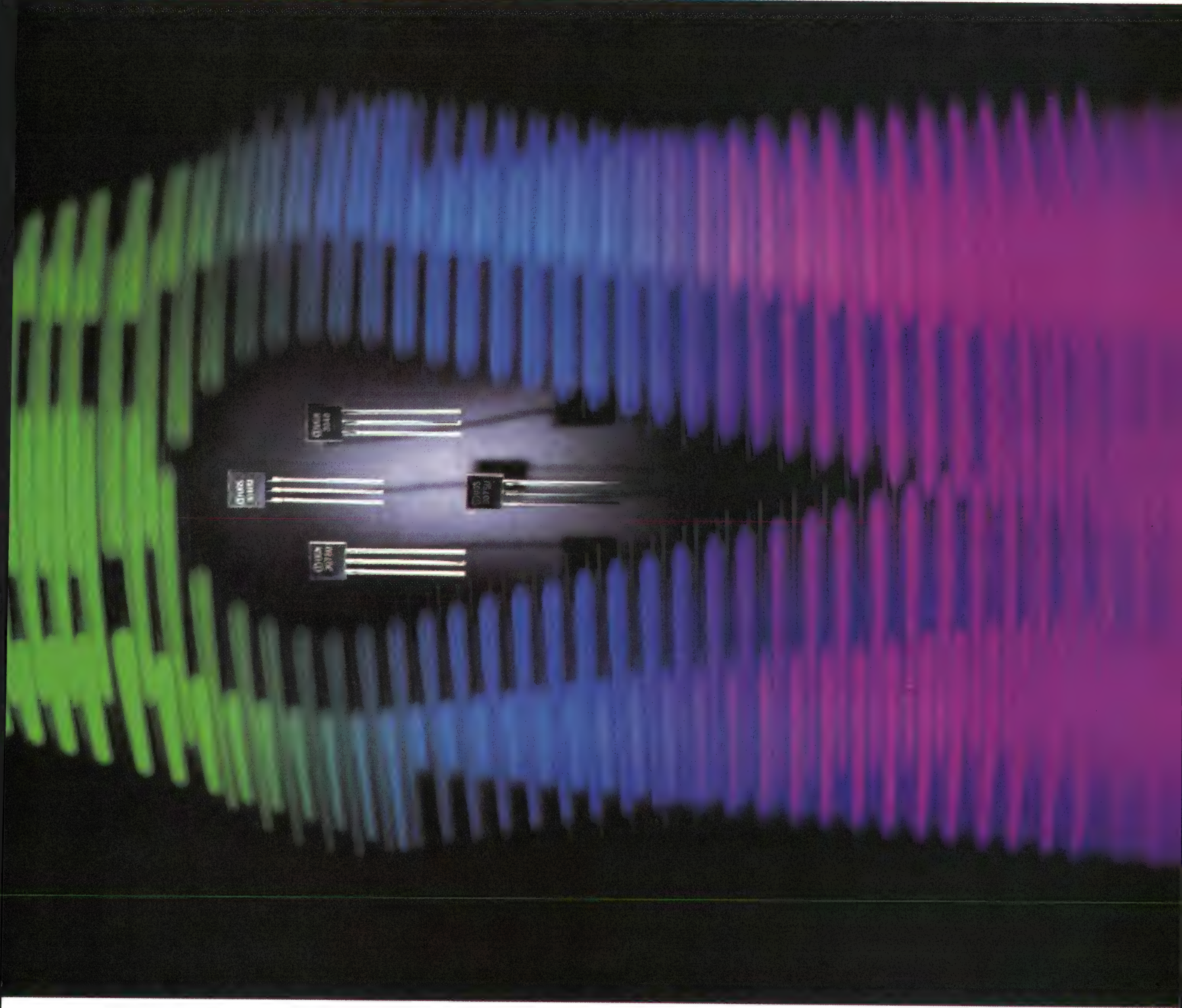

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CIRCLE NO 73

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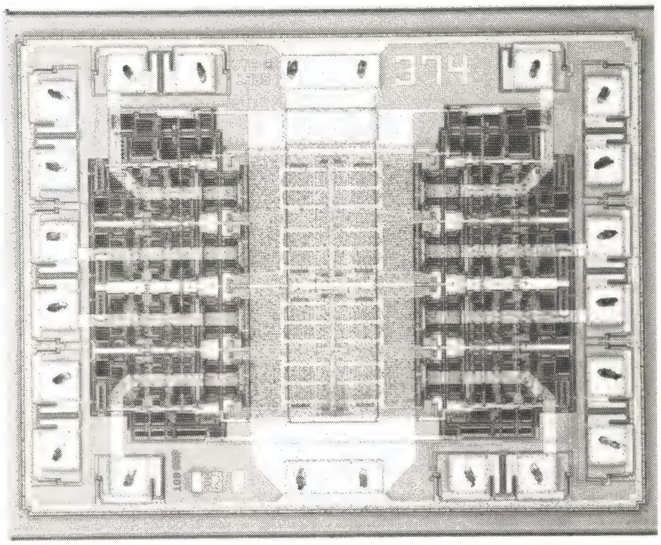
Despite requiring a lot of power, ECL logic devices furnish more cost-effective interfaces for supercomputer systems than GaAs or CMOS parts.



Operating at ECL speeds with a typical propagation delay of 6 nsec, *VTC's V54/74ACT374 CMOS octal edge-triggered D flip-flop works with a 3-state data bus and conventional 5V TTL circuitry. The part draws 48 mA max of supply current.*

that operate at speeds in the neighborhood of 50 MIPS.

On the other hand, CMOS is preferable when you want to handle designs involving computation-intensive processes for which speed is not critical, or for which the speed you require can be achieved through other design choices. Your decision to use CMOS logic will depend mainly upon your ultimate system design. Parallel-processing computers, for example, favor higher density CMOS chips and achieve their staggering speeds through innovations in computer architecture.

Faster-than-ever CMOS rivals ECL speeds

Although CMOS has been steadily approaching typical ECL speeds, the key advantage of CMOS is still its ability to handle complex logic functions. Low power dissipation per gate enables CMOS logic to achieve the circuit densities that handle this complexity. Today's CMOS MSI-logic ICs already exceed the performance of any standard TTL chip on the market. You can now buy standard CMOS glue logic that runs at clock speeds above 100 MHz from Integrated Device Technology, Performance Semiconductor, Toshiba, and VTC.

Tom Longo, president of Performance Semiconductor and former engineering director for the development of F100K ECL chips at Fairchild, maintains that the growth of ECL ICs will be limited by the growth of high-speed CMOS logic chips. Within a few years, he believes, CMOS will crowd GaAs as well. Performance Semiconductor's CMOS flip-flops, which toggle at 300 MHz, constitute some evidence for this prediction. Longo disagrees with assertions that ECL will be able to attain the densities of CMOS logic parts.

CMOS-family clock speeds reach 250 MHz

Using a 0.8-μm process, Performance Semiconductor has created a family of low-power CMOS logic devices that toggle at 250 MHz, including the P54/74PCT273/374 flip-flops and the P54/74PCT373/573 gated latches. The company's P54/74 ICs drive a 64-mA line over commercial temperature ranges. The flip-flops and latches both come in 20-pin plastic DIPs for $1.96 or ceramic DIPs for $3.95 (100).

This month, Toshiba America will be offering samples of its TC74AC Series CMOS logic ICs, which run at clock frequencies as high as 150 MHz. The company's CMOS glue-logic parts operate over the −40 to +85°C temperature range, and they're intended as pin-compatible replacements for Fairchild's line of Fast TTL ICs.

Other companies are making CMOS logic devices that operate in the 100-MHz region and meet MIL-STD-883C specs as well. Last March, IDT unveiled its 39C800 Series high-speed CMOS logic ICs, made with the company's proprietary 1.2-μm CEMOS process. Unlike many standard CMOS glue-logic chips, IDT's ICs furnish both TTL and CMOS I/O compatibility, low input capacitance (6 to 8 pF typ), high output-drive capability, and limited power dissipation (5 μW max).

The 39C800 Series devices are pin compatible with AMD's Am29800 9-bit I/O architecture. They spec a propagation delay of 7.5 nsec, and they provide the address/data paths required in applications that employ parity bits, such as high-speed graphics. The first members of the series were the IDT39C823 bus-interface register, the -39C843 bus-interface latch, and the -39C863 bus tranceiver. All three parts come in 24-pin DIPs and cost $5.90 (100).

AMD introduced its own CMOS versions of the Am29800 Series TTL chips in June: the Am29C821 10-bit bus-interface register and the Am29C843 9-bit bus-interface latch. These devices have the same 24-mA drive capability as their bipolar counterparts, but with less than 20% of the power dissipation. Commercial versions of both chips come in 24-pin plastic DIPs and cost $2.20 (100). Military versions of these devices are available in sample quantities.

In addition to IDT, Fairchild, RCA, and VTC are offering CMOS glue-logic chips that furnish clock rates in the 100-MHz range and meet MIL-STD-883C stan-

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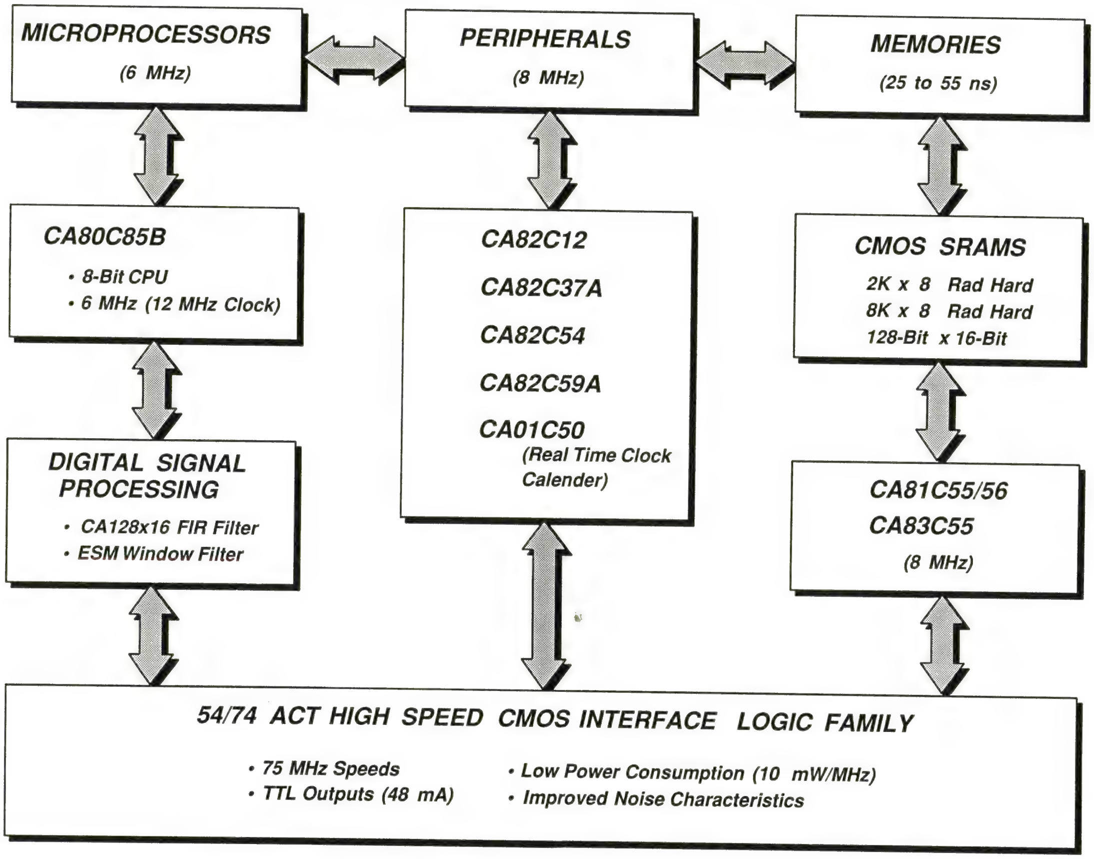

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Circle No 704

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dards. In May, Fairchild and RCA received approval from the Defense Electronics Supply Center (DESC) for initial members of their 54ACXXXDMQB (Fact) and CD54HCTXXXF/3A (QMOS) series, respectively. RCA has already received DESC qualification for 40 of its QMOS glue-logic parts, while Fairchild expects to have about 30 more of its Fact chips certified by the DESC by the year's end.

Improved noise immunity

Last fall, VTC introduced the first 20 of its planned 50 1.6-μm CMOS V54ACTXXX glue-logic devices, including 8-, 9-, and 10-bit buffers, latches, flip-flops, and tranceivers. All parts come in 20- and 24-pin DIPs. Besides providing improved noise immunity compared with conventional TTL glue logic, input circuits to VTC's V54- and V74ACTXXX parts can withstand 2000V of ESD. Typical quiescent power dissipation for all of these DESC-approved parts is 5 μW.

The fastest members of VTC's V54/74ACTXXX Series spec typical propagation delays of 6 nsec. These parts include the -373/74 and -575/80 octal 3-state D flip-flop/latches. The -3XX parts come in 20-pin DIPs, small-outline IC packages, LCCs, or PLCCs, and they cost $1.67 (100). The -5XX chips come in 24-pin DIPs or small-outline IC packages, or in 28-pin PLCCs, and they cost $2.08 (100). Like IDT, VTC makes pin-compatible CMOS versions of the Am29800 family. These parts cost $2.55 (100).

CMOS programmable-logic chips still run more slowly than either TTL PALs or individual standard CMOS glue-logic components. For instance, CMOS versions of MMI's 12-nsec TTL PAL20 Series, made by Cypress Semiconductor and Sprague Solid State, only deliver 25-nsec propagation delays. Nevertheless, both of these 24-pin, UV-erasable CMOS PALs drop supply-current requirements from approximately 200 to 55 mA max. Cypress's PLDC20G10-25PC sells for $11.25 (100); Sprague's SPL16RCxQ-25 costs $7.95 (1000).

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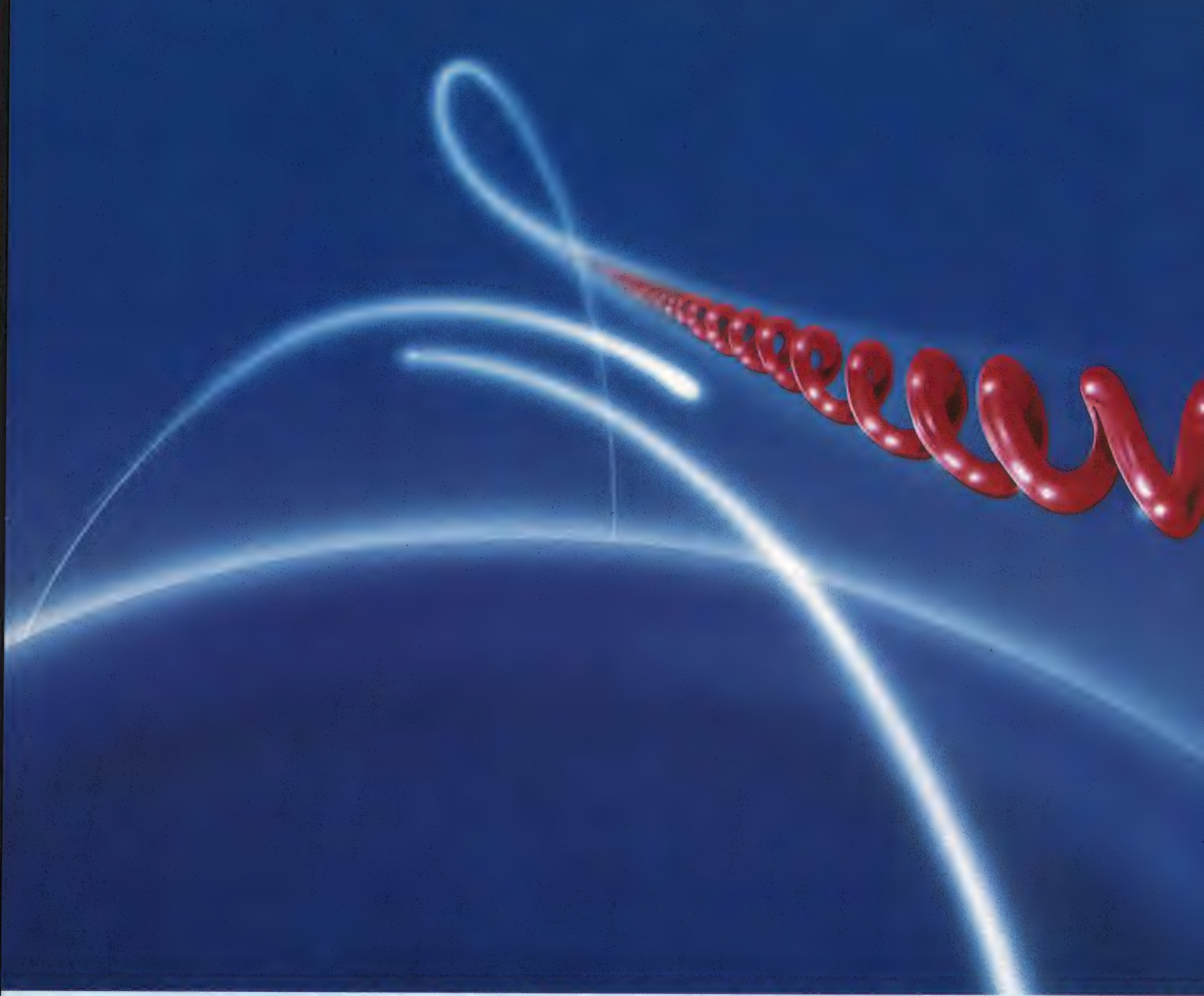

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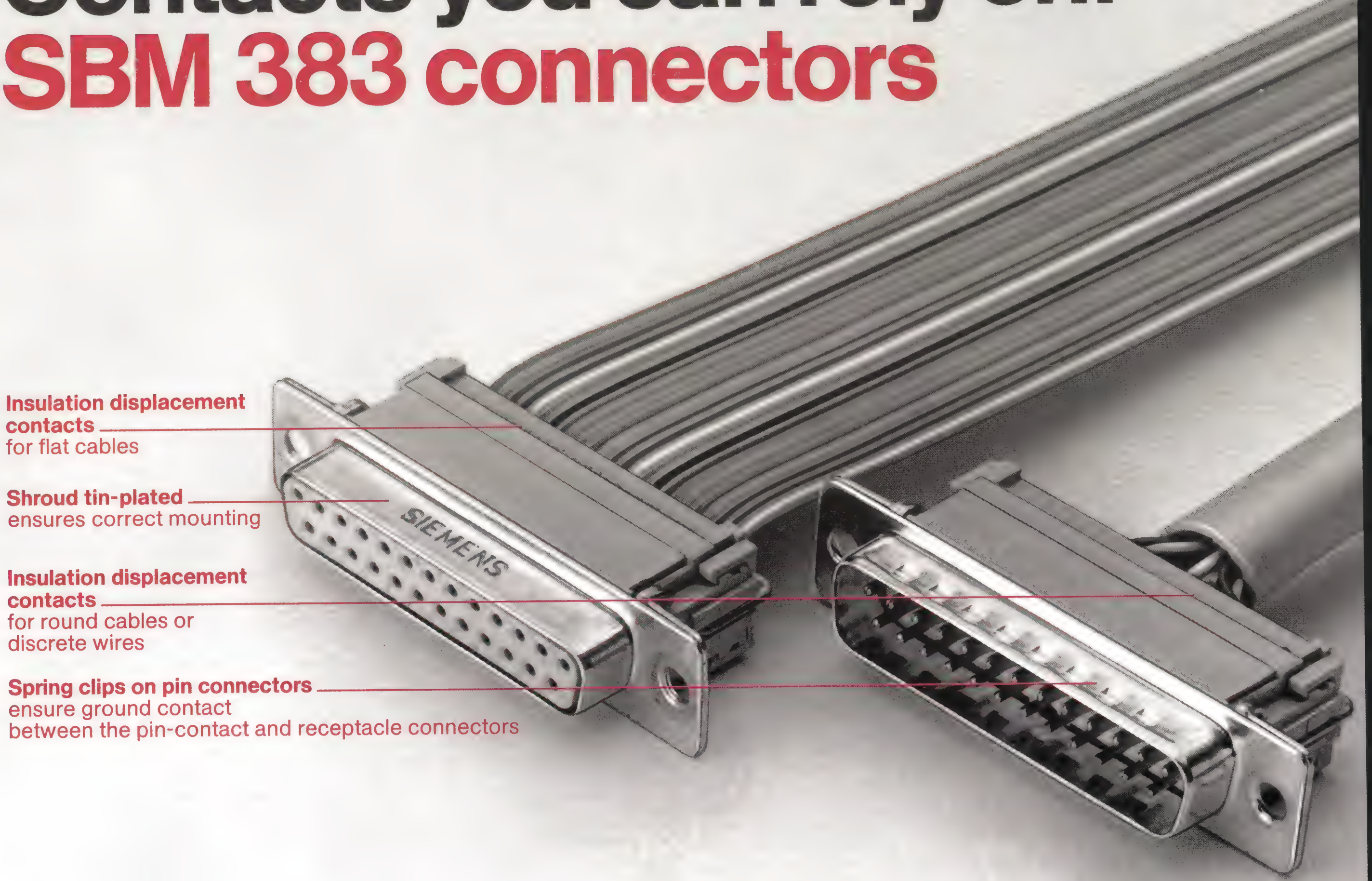
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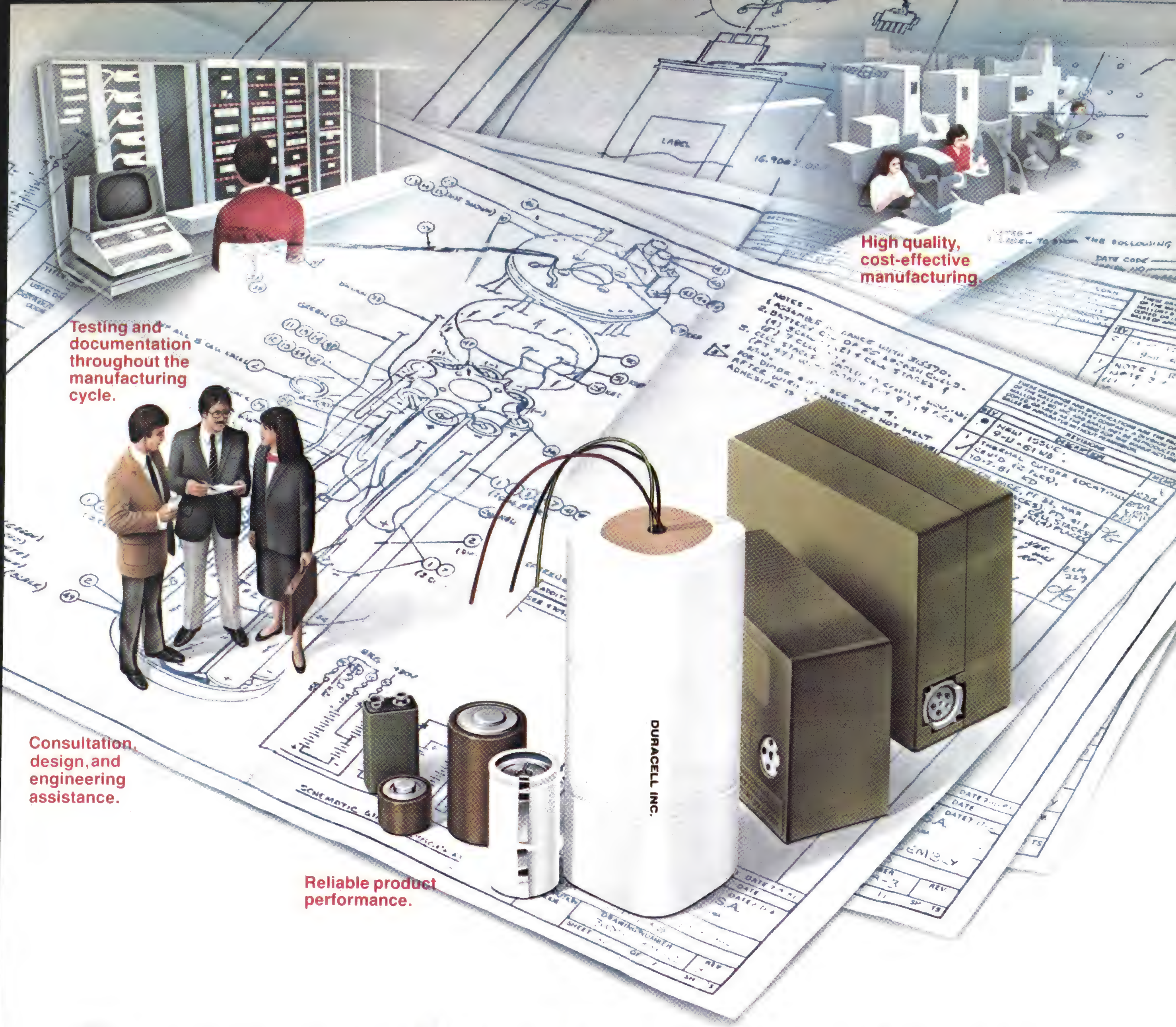

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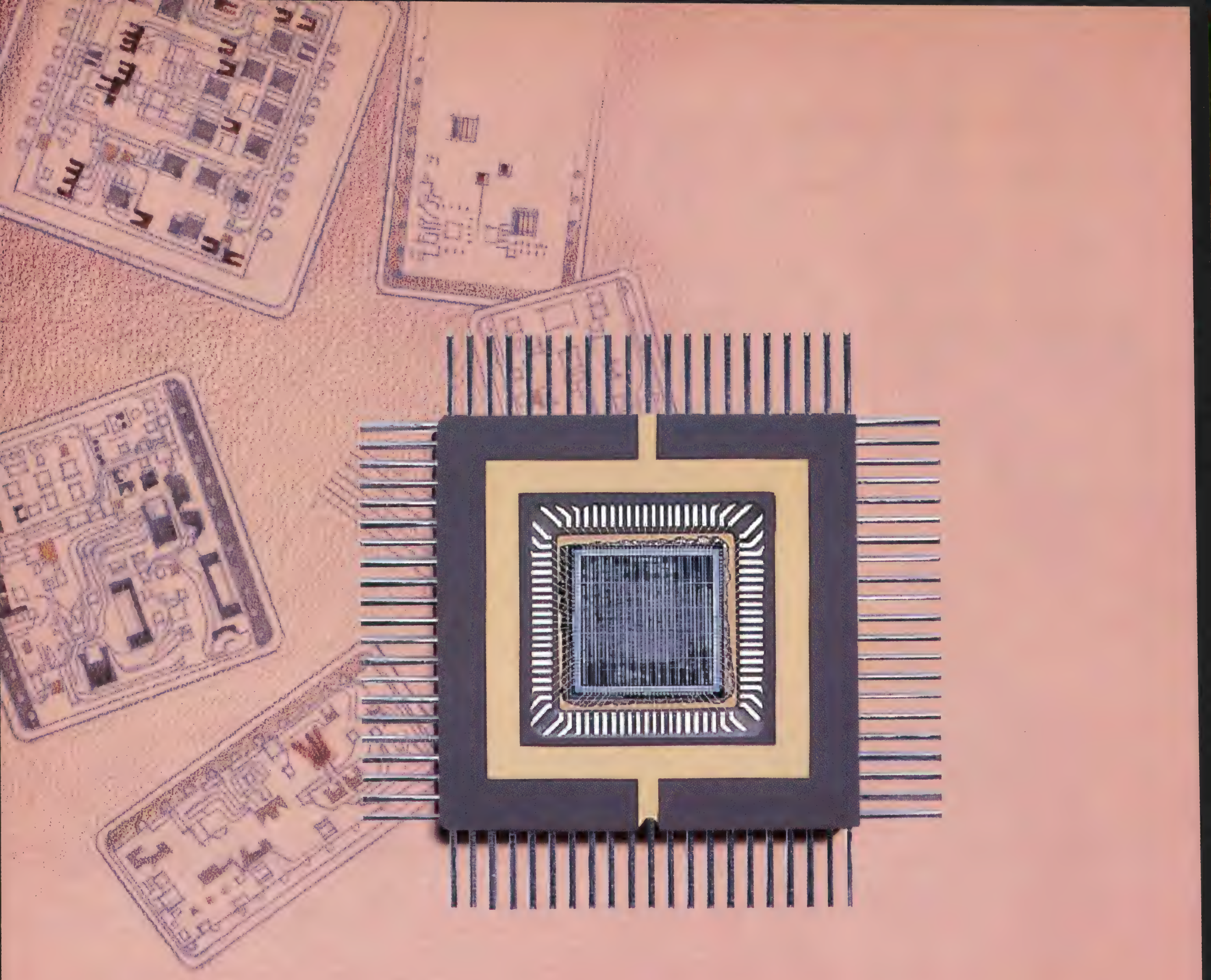

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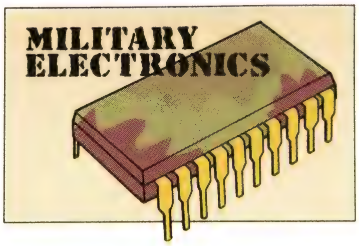


Examine and verify GaAs IC performance

By applying appropriate input signals, employing a sampling scope, and using certain techniques, you can measure the propagation delays and setup and hold times of GaAs chips and corroborate your vendor's specs.

Louis Pengue, *TriQuint Semiconductor*,
and Eldon Walters, *Tektronix*

To test a GaAs chip's propagation delay and setup and hold times, you must set up a lab arrangement with three main characteristics. First, you must provide suitable input signals that have sufficient slew rate and amplitude. Second, you must have access to an appropriate test fixture. Third, you must set your sampling scope to capture the input and output test signals and make comparisons. You have a choice of procedures for using the scope, depending on the capabilities of your instrument.

Determining a GaAs device's propagation delay is relatively easy if your sampling scope can detect such short delays (hundreds of picoseconds). Setup and hold measurements, on the other hand, prove difficult because you must precisely adjust the time between the test-clock and data signals so that an output ambiguity results. By finding the exact point at which the output makes the transition to an ambiguous state, you can determine setup and hold values.

Of the three parts of your test setup, applying the input signals can be the trickiest. The three inputs—clock, data, and scope trigger—must be in sync with each other. As a basis for these signals, an RF signal source produces sine waves varying between 100 and 1000 MHz. Testing occurs at relatively low frequencies to ensure steady-state operation of the GaAs circuits.

Although the RF generator's sine-wave output is the basis of the input-signal part of the test system, you can't use its output directly at the selected measurement frequencies because its rise time is too slow. The slow rise time (reflected in a low slew rate) would result in unrepeatable results because it's difficult to determine precisely when the digital-switching threshold is crossed. The slow rise time of the sine wave can also cause erratic operation of the GaAs digital IC.

A square-wave generator produces signals with fast rise times, but a generator that can produce appropriate square waves or pulse trains at the desired measurement frequencies (100 to 500 MHz) doesn't exist. Some pulse generators offer an adequate repetition rate, but they don't produce the necessary 1 to 2V p-p amplitude. If GaAs chips' I/O signals are ECL compatible, then their logic threshold is −1.3V, their minimum input logic signal is 400 mV (−1.1 to −1.5V), and their

Setup and hold measurements prove difficult because you must precisely adjust the time between test-clock and data signals so that an output ambiguity results.

minimum output logic signal is 600 mV (−1.0 to −1.6V). Nevertheless, you need a full 1V p-p clock to drive the device at maximum frequency.

Use GaAs chip for input signals

Fortunately, you can use a GaAs device (other than the one under test) to square-up the sine wave and to separate the single input into the three signal components needed in the test. The RF generator drives a GaAs chip that provides signals to the GaAs chip under test. The output of the first GaAs chip provides a high enough slew rate (about 250-psec rise and fall times) to ensure that variability in threshold switching is no longer a problem and that the device under test operates properly.

You can, of course, use a microwave power divider to split the clean clock signal from the conditioning circuit into test-clock and scope-trigger signals. However, this approach results in too much degradation of the signal's amplitude because the divider is a passive device that simply divides the available power between its two output signals.

Instead, you should route the clean input clock through two paths consisting of GaAs inverters. The signals that emerge are in sync and at full amplitude. One of the signals serves as the test clock, and the other serves as the basis for the test data. You can use virtually any GaAs inverters (or indeed any GaAs devices) to produce this desired result; **Fig 1** shows the inverters in TriQuint's Q-Chip evaluation device. To generate the test-data signal, you can route one of the outputs from the inverter strings to a GaAs divide-by-4 circuit. The divider's noninverted output then serves as a data signal (pin 40) while the inverted output (pin 42) triggers the scope **(Fig 2).**

The next requisite part in the lab setup is a standard test fixture, which includes an evaluation board and a chip-socket assembly. In particular, the socket should accept a 48-pin chip carrier and incorporate coplanar 50Ω signal lines from the die site to interconnection pads at the socket substrate's edge. Also, a beryllia substrate will minimize thermal gradients, and using four integral, 1000-pF power-supply bypass capacitors will minimize digital switching noise.

The test fixture's through-board screws fasten the socket and its heat sink to a ceramic/PTFE (polytetrafluoroethylene) composite-laminate test board with a dielectric constant of 10.6. Signals from the IC under test travel to the edge of the board along 0.010-in.-wide traces that appear as 50Ω signal lines. Finally, elastomeric connectors form the interconnect from the chip carrier to the test board.

After input signals and a test fixture, the remaining element in your setup is the instrumentation. To adequately characterize a GaAs chip, the test equipment must be able to resolve time increments of approxi-

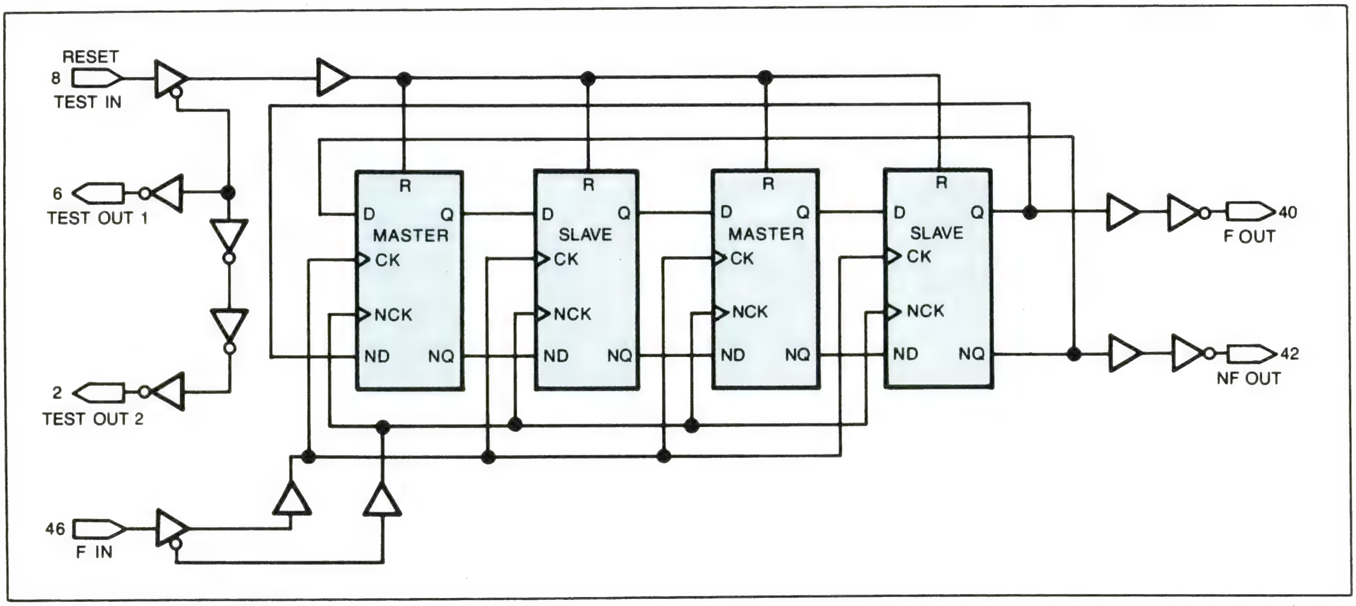
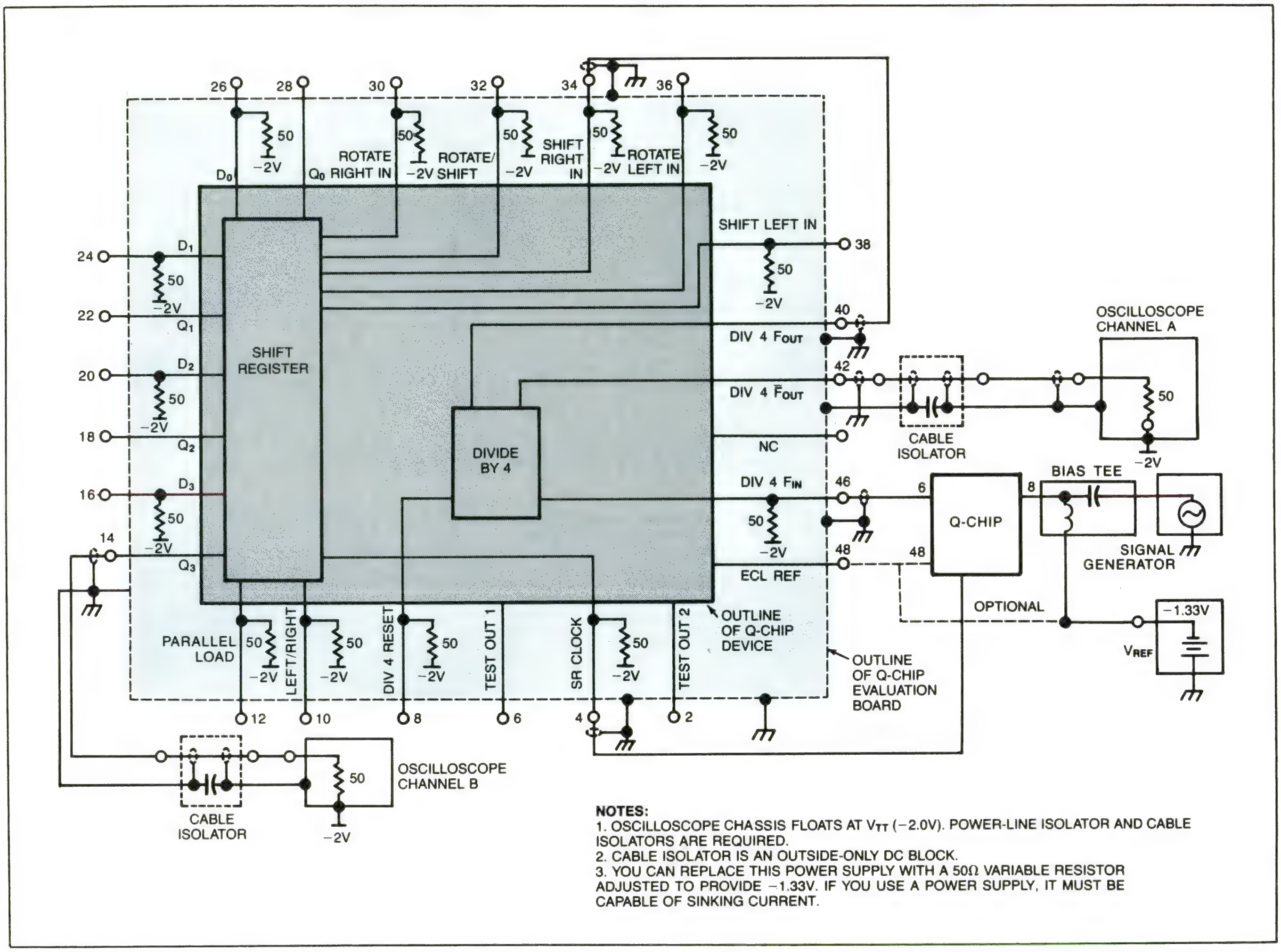


Fig 1—You can use inverters from one GaAs IC *to create square pulses for the GaAs IC under test. The Test Out line (pin 2) drives the test-clock signal, and the divide-by-4 circuit creates the test-data signal.*



NOTES:

1. OSCILLOSCOPE CHASSIS FLOATS AT V_{TT} (−2.0V). POWER-LINE ISOLATOR AND CABLE ISOLATORS ARE REQUIRED.
2. CABLE ISOLATOR IS AN OUTSIDE-ONLY DC BLOCK.
3. YOU CAN REPLACE THIS POWER SUPPLY WITH A 50Ω VARIABLE RESISTOR ADJUSTED TO PROVIDE −1.33V. IF YOU USE A POWER SUPPLY, IT MUST BE CAPABLE OF SINKING CURRENT.

Fig 2—In this test setup, *the divider's noninverted output is the basis for the data signal while the inverted output triggers the scope.*

mately 10 psec and to produce repeatable results within approximately 30 psec.

In the test setup in **Fig 2,** a Tektronix sampling oscilloscope provides the necessary resolution. It comprises a 7854 mainframe with a 7T11A sampling sweep plug-in unit and a 7S11 sampling unit with S6 sampling heads. The 7S11 with S6 sampling heads is capable of capturing rise times as small as 30 psec. The 7T11A has a 10-psec/div calibrated timebase with a timing accuracy within 3%.

When making measurements to determine propagation delay, you can take two approaches to using a sampling scope. One method is to use two of the scope's channels to capture the input and output signals simultaneously. Circuitry in the test setup introduces delays dependent on each particular channel. Before taking measurements, you need to calibrate the system to account for differences in scope-channel delay in addition to delay between the test fixture and the scope.

The second approach eliminates the necessity for calibrating input channels. Employing one of the scope's channels, you can sample the input signal, using the separate synchronized trigger produced by the conditioning IC's inverter string to tell the scope when to acquire the signal. You can then use the same scope probe on the same channel to sample the output signal, using the same trigger that you used for the first sample. With the two signals stored in the 7854's memory, you use the scope's Δt capability to determine the propagation delay. Because the same wire delays are involved in both parts of the procedure, they don't affect the actual values measured.

TABLE 1—INTERPRETATION OF MEASURED DATA

SYMBOL	EDGE AMBIGUITY	DATA HIGH	DATA LOW
t_F	FALLING	$-t^{H}_{HOLD}$	$t^{L}_{SET\text{-}UP}$
t_R	RISING	$t^{H}_{SET\text{-}UP}$	$-t^{L}_{HOLD}$

NOTE:
t_F AND t_R MAY BE NEGATIVE IF THE CLOCK EDGE LEADS THE DATA EDGE.

You also have a choice of approaches for measuring setup and hold times. In one approach, you adjust the interval t_F between the clock and data-in edges until the output data becomes ambiguous—you're not sure on which clock transition the output is changing. At that point, you read t_F from the scope as either the setup or hold time, depending on the test setup **(Table 1).** This procedure is difficult to perform at the frequencies used to test GaAs devices, and it demands the use of two scope channels.

A second, and easier, method for performing setup and hold measurements involves adjusting the t_F interval by changing the RF generator's frequency. Because the data input trails the clock input by a fixed interval (the propagation delay of the frequency divider), t_F varies as the clock frequency varies. In essence, you can change the frequency to change setup and hold conditions. As before, monitoring the output of the device under test allows you to determine where the signal becomes ambiguous. You can then use the other scope channel to read the setup or hold time, or you can employ the single-channel approach used for propagation-delay measurements.

Fig 3 illustrates this setup and hold measurement approach. The device under test latches data on the clock's falling edge. **Fig 3a** shows an unambiguous state where the first clock transition after the data transition latches the data after the falling transition. As you increase the clock's frequency, however, and the clock and data edges get closer together, you eventually reach a point where the second falling clock edge after the data edge triggers the device **(Fig 3b).** Between these two states is a condition where a transitional state exists **(Fig 3c)**—the ambiguous state that indicates where the device's setup and hold requirements are barely met. You can recognize this ambiguous state by noting the point at which it's difficult to tell whether the first or second clock after the data edge is triggering the device.

A sample characterization demonstrates how you can measure propagation delay and setup and hold times. The device under test is a shift register in TriQuint's GaAs evaluation chip **(Fig 4);** it operates at clock speeds ranging to 1.8 GHz. The evaluation chip combines divide-by-4 and 4-bit universal shift-register circuits. The techniques described here characterize the IC's shift register, but the procedure is generalized so it can apply to other digital GaAs devices.

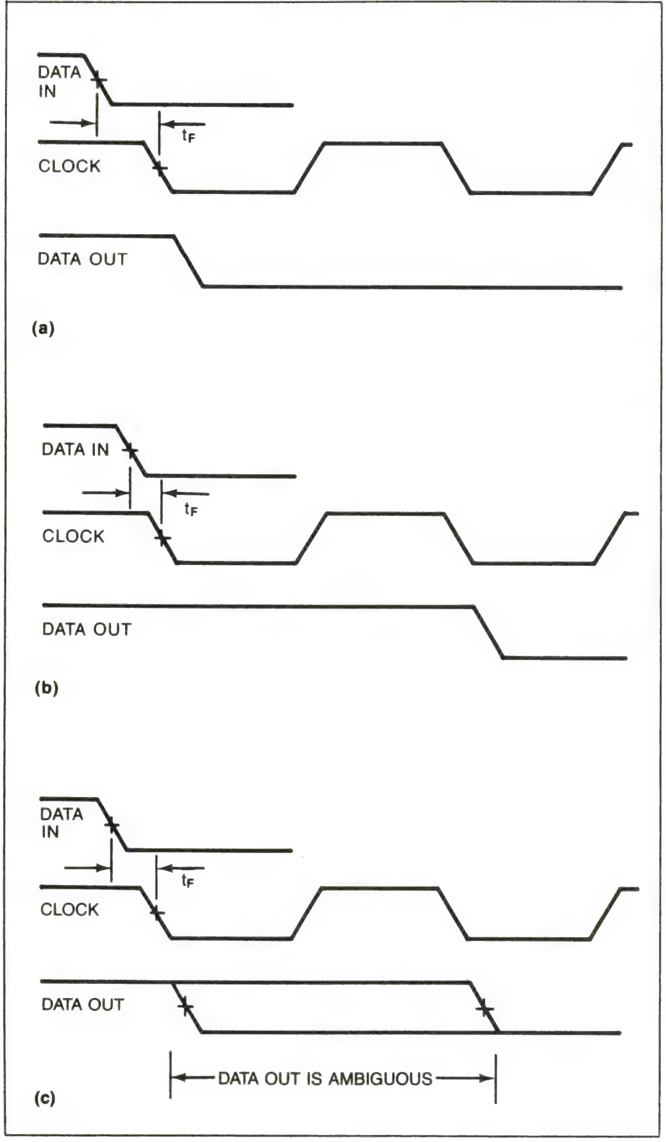


Fig 3—Adjusting the interval between clock and data signals *lets you determine the setup and hold times for your GaAs IC.*

Some pulse generators offer an adequate repetition rate to test GaAs ICs, but they don't produce the necessary 1V p-p amplitude.

To match manufacturing specs, you'd have to test a nominal device from a nominal wafer—one where every one of the many process variables is at the mean. This matching is virtually impossible, of course, so you simply expect to find actual propagation-delay values within a reasonable tolerance of the calculated ones (for ICs, a 10% tolerance is considered normal). Nonetheless, the actual values should certainly be within the manufacturer's worst-case specs.

As you take measurements on your device, you need to subtract the delay of the wiring on the board from the total signal delay to find the delays on the GaAs chip. To make the calculated and actual propagation delays comparable, you can employ time delay reflectometry (TDR) to find the wiring delays and add results to the calculated delay values. **Table 2** includes the TDR results and shows the final calculated values for the expected propagation delays when using a Tektronix 7S12 TDR plug-in unit in the 7854 scope with an S6 sampling head and an S52 pulse generator head. Because some of the output pins are closer than others, the wiring delay values differ, depending on the output.

First, establish an estimate of the propagation-delay values you expect to find, based on information from the GaAs device's manufacturer or based on circuit simulations. In the case of an off-the-shelf GaAs IC, the device manufacturer should supply delay information. If this is the case, your characterization then simply involves verifying a data-sheet value.

In semicustom ICs, however, the propagation delay depends on how you configure the chip. You have to sum the delay values of each internal component in a specific signal path to arrive at an estimate for overall propagation delay. The device manufacturer should supply approximate delay values for the internal components, but the load on each component's output

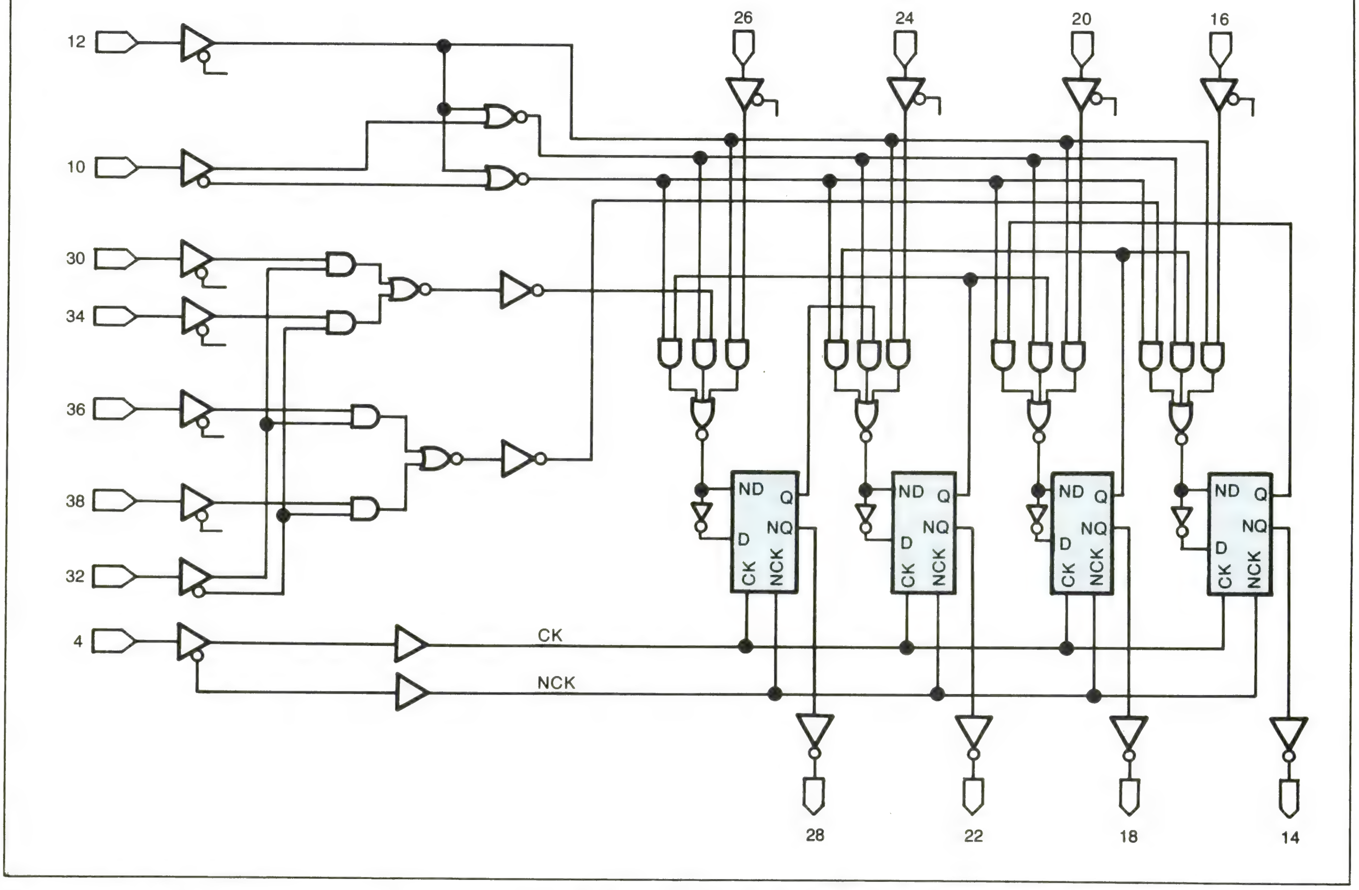


Fig 4—Here, a shift register *that resides on a GaAs semicustom IC serves as the device under test. In addition to the shift-register circuits, the chip contains divide-by-4 counters.*

To adequately characterize a GaAs chip, your test equipment must be able to resolve 10-psec time increments and produce repeatable results within about 30 psec.

changes depending on how you configure the chip, which in turn changes each component's propagation delay. In such cases, either a simulation of the logic-element models or the logic-element data sheet provides the specifications you need. The logic models' timing information comes from Spice circuit simulations of the logic circuits.

In the sample device under test (**Fig 4**), the clock signal's propagation path includes four components. From the clock input (pin 4) to one of the data outputs (say, pin 28), the delay components include an input cell, a buffer, one of the shift register's flip-flops, and an output cell. According to the Q-Chip's data sheets, the delays for the first three components are approximately 140, 90, and 140 psec, respectively. The output buffer's delay depends on whether the signal edge is rising (150 psec) or falling (250 psec). The overall clock-to-Q propagation delay is thus 520 or 620 psec for a rising or falling edge, respectively.

At this point in the procedure, finding the actual propagation delay is just a straightforward matter of taking measurements. **Table 3** lists the values obtained for the sample device under test. For each of the shift register's outputs, **Table 3** includes four sets of delay values. The waveform in **Fig 5** shows one measurement of the delay from the shift register's rotate-right input to its Q_0 (falling) output.

Taking several measurements of the propagation delay of the device under test ensures the validity of the data. For valid data, the measurements should be roughly equivalent, which is the case. An average of the measured values gives you the most accurate indication of the actual experimental propagation delay. The Δt value represents the difference in propagation delay between a rising edge and a falling edge.

Table 3 includes two sets of total delay averages: one for each group of data input paths and one for each group of output paths. Corrected for wiring delays, the overall average rising and falling delay values are 462

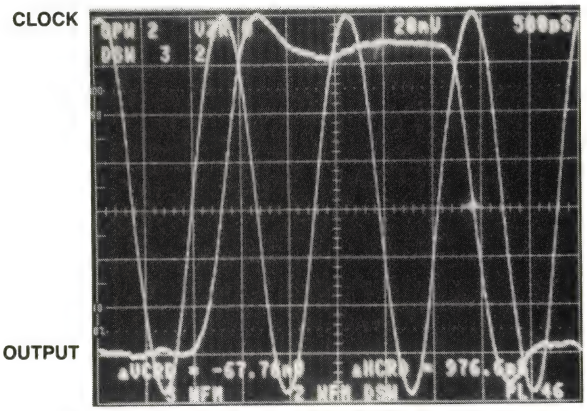


***Fig 5—The propagation delay for the GaAs shift register** appears as the 976-nsec interval between the falling edge of the clock signal and the falling edge of the output.*

TABLE 2—CALCULATION OF TOTAL PROPAGATION DELAY

BOARD DELAY:

TDR DELAY MEASURED FROM SMA CONNECTOR ON EVALUATION BOARD TO BOND PAD ON Q-CHIP DIE.

SHIFT REGISTER CLOCK INPUT DELAY = 240 pSEC
SHIFT REGISTER Q_0 OUTPUT DELAY = 240 pSEC
SHIFT REGISTER Q_1 OUTPUT DELAY = 240 pSEC
SHIFT REGISTER Q_2 OUTPUT DELAY = 380 pSEC
SHIFT REGISTER Q_3 OUTPUT DELAY = 390 pSEC

EXPECTED MEASUREMENT DELAY:

MEASUREMENT DELAY (SMA INPUT TO SMA OUTPUT) = SHIFT REGISTER CLOCK INPUT DELAY + IC PATH DELAY + Q_N OUTPUT DELAY

OUTPUT RISING
Q_0 DELAY = 240 pSEC + 520 pSEC + 240 pSEC = 1000 pSEC
Q_1 DELAY = 240 pSEC + 520 pSEC + 240 pSEC = 1000 pSEC
Q_2 DELAY = 240 pSEC + 520 pSEC + 380 pSEC = 1140 pSEC
Q_3 DELAY = 240 pSEC + 520 pSEC + 390 pSEC = 1150 pSEC

OUTPUT FALLING (ADD 100 pSEC)
Q_0 DELAY = 1100 pSEC
Q_1 DELAY = 1100 pSEC
Q_2 DELAY = 1240 pSEC
Q_3 DELAY = 1250 pSEC

TABLE 3—CLOCK-TO-Q PROPAGATION DELAY (pSEC)

OUTPUT RISE/ FALL	BOARD DELAY	MEASURED DELAY ON BOARD				ADJUSTED FOR BOARD DELAY					
		SHIFT-RIGHT IN	ROTATE-RIGHT IN	SHIFT-LEFT IN	ROTATE-LEFT IN	SHIFT-RIGHT IN	ROTATE-RIGHT IN	SHIFT-LEFT IN	ROTATE-LEFT IN	Q AVG	F-R Δt
Q_0 RISE	480	966	937	908	918	486	457	428	438	452	
Q_0 FALL	480	1094	1035	1055	1045	614	555	575	565	577	125
Q_1 RISE	480	976	966	966	976	496	486	486	496	491	
Q_1 FALL	480	1065	996	1045	1065	585	516	565	585	562	71
Q_2 RISE	620	1094	1074	1084	1065	474	454	464	445	459	
Q_2 FALL	620	1221	1172	1143	1133	601	552	523	513	547	88
Q_3 RISE	630	1084	1035	1094	1104	454	405	464	474	449	
Q_3 FALL	630	1200	1182	1201	1201	570	552	571	571	566	117
PATH AVERAGE RISING						477	450	460	463	462	
PATH AVERAGE FALLING						592	543	558	558	562	100
Δ t FOR PATH AVERAGE						115	93	98	95	100	

THIS DATA IMPLIES:

CLOCK-TO-Q IC DELAY:
Q RISING = 462 pSEC
Q FALLING = 562 pSEC
Δ t = 100 pSEC

FOR A SECOND IC:

CLOCK-TO-Q IC DELAY:
Q RISING = 560 pSEC
Q FALLING = 678 pSEC
Δ t = 118 pSEC

SPICE PREDICTED:

Q RISING = 520 pSEC
Q FALLING = 620 pSEC
Δ t = 100 pSEC

and 562 psec, respectively. The average Δt (t_R minus t_F) for both sets of averages equals 100 psec. These delay figures agree closely with predicted delay values, and the predicted and measured Δt values are identical.

The extremely close agreement between the expected and actual data implies that the timing models are accurate. Just to make sure, though, it's wise to perform measurements on another Q-Chip. In this example, the results are as follows: t_R=560 psec, t_F=678 psec, and Δt=118 psec. The average of the measured values from these two chips comes very close to the Spice-predicted delays.

Characterize setup and hold times

The final part of the characterization process is to measure setup and hold values. For the shift register in **Fig 4,** the setup and hold times are those of the flip-flops, which constitute the only clocked components in the circuit.

To obtain accurate estimates of what the values should be, you must strip away from your measured delays the delays associated with all the chip elements except the flip-flops. As with the propagation-delay estimates, you sum the simulated delay values for these other elements in the signal path. For the shift register, consider four sets of delay paths: the path from the rotate/shift, left/right inputs; the path from the parallel load input; the path from the parallel data inputs; and the path from the clock input.

TABLE 4—IC PATH DELAY ESTIMATES (pSEC)

INPUT CLOCK PATH, HIGH-TO-LOW:

SHIFT REGISTER CLOCK INPUT = 140 + 94 = 234 pSEC

INPUT DATA PATHS, LOW-TO-HIGH:

ROTATE/SHIFT AND LEFT/RIGHT INPUTS = 155 + 130 + 95 + 153 = 533 pSEC
PARALLEL LOAD CONTROL INPUT = 225 + 178 = 403 pSEC
D_0:D_3 INPUTS = 155 + 153 = 308 pSEC

INPUT DATA PATHS, HIGH-TO-LOW (ADD 95 pSEC):

ROTATE/SHIFT AND LEFT/RIGHT INPUTS = 628 pSEC
PARALLEL LOAD CONTROL INPUT = 498 pSEC
D_0:D_3 INPUTS = 403 pSEC

TOTAL IC DELAY ADJUSTMENT:
THIS DELAY = INPUT DATA PATH DELAYS − INPUT CLOCK DELAY

INPUT DATA PATHS, LOW-TO-HIGH:

ROTATE/SHIFT AND LEFT/RIGHT INPUTS = 533 − 234 = 299 pSEC
PARALLEL LOAD CONTROL INPUT = 403 − 234 = 169 pSEC
D_0:D_3 INPUTS = 308 − 234 = 74 pSEC

INPUT DATA PATHS, HIGH-TO-LOW (ADD 95 pSEC):

ROTATE/SHIFT AND LEFT/RIGHT INPUTS = 394 pSEC
PARALLEL LOAD CONTROL INPUT = 264 pSEC
D_0:D_3 INPUTS = 169 pSEC

One other factor—the logic state of the signal into the flip-flop—affects the data delay to the shift register. In **Fig 4,** each flip-flop in the shift register has positive and negative data inputs (D and ND). The ND input comes directly from the preceding logic gate, but

One method for setup and hold measurement involves adjusting the t_F interval by changing the RF generator's frequency.

the D input results from an inverter between ND and D. Because of the flip-flop's logic design, a low-to-high transition at ND can immediately start to propagate through the flip-flop without waiting for the opposite transition to take place at the D input. However, if a high-to-low transition appears at ND, the data won't propagate through the flip-flop until the transition reaches the D input through the inverter. The overall delay for a high-to-low transition is thus lengthened by the inverter's propagation delay. This condition influences the delays that are used to adjust the measured setup and hold data.

Table 4 lists all the estimated delay values and the final correction values that you subtract from the measured setup and hold times to determine valid setup and hold times. The measured values for setup and hold appear in **Table 5.** The final setup time for the overall IC should equal the flip-flop setup time plus the added input gate delay minus the clock delay. Therefore, as with the propagation-delay measurements, you subtract the wiring delay from the measured delay; this time, however, the wiring delays affect both clock and data lines, so you only subtract the difference between a data line and the clock signal. Two of the inputs thus have a zero correction factor because both the data and clock paths entail equal delays.

For a measurement of a single data transition, the setup and hold times should exhibit a symmetrical relationship. More concisely, the magnitude of a data=high setup time should equal the magnitude of a data=low hold time, but the hold time is negative. The hold time for the GaAs IC equals the flip-flop hold time

TABLE 5— DERIVED FLIP-FLOP SETUP VALUES (pSEC)

INPUT PATH	MEASURED DATA SETUP TIME D=1	MEASURED DATA SETUP TIME D=0	BOARD DELAY WRT CLOCK	BOARD DELAY ADJUSTED DATA D=1	BOARD DELAY ADJUSTED DATA D=0	IC PATH DELAY D=1	IC PATH DELAY D=0	DERIVED DATA FOR FLIP-FLOP D=1	DERIVED DATA FOR FLIP-FLOP D=0
SHIFT RIGHT	645	492	0	645	492	299	394	346	98
ROTATE RIGHT	702	844	130	572	714	299	394	273	320
SHIFT LEFT	725	861	160	565	701	299	394	266	307
ROTATE LEFT	644	927	160	504	767	299	394	205	373
PARALLEL LOAD	610	839	160	450	679	169	264	281	415
D_0	444	581	160	284	421	74	169	210	252
D_1	507	649	160	347	489	74	169	273	320
D_2	434	629	130	304	499	74	169	230	330
D_3	234	498	0	234	498	74	169	160	329
							MEAN =	249	304

THIS DATA IMPLIES THE BASIC FLIP-FLOP SETUP/HOLD TIMES ARE APPROXIMATELY:
D = HIGH SETUP = 250 pSEC, D = 0 HOLD = −250 pSEC;
D = LOW SETUP = 300 pSEC, D = 1 HOLD = −300 pSEC.

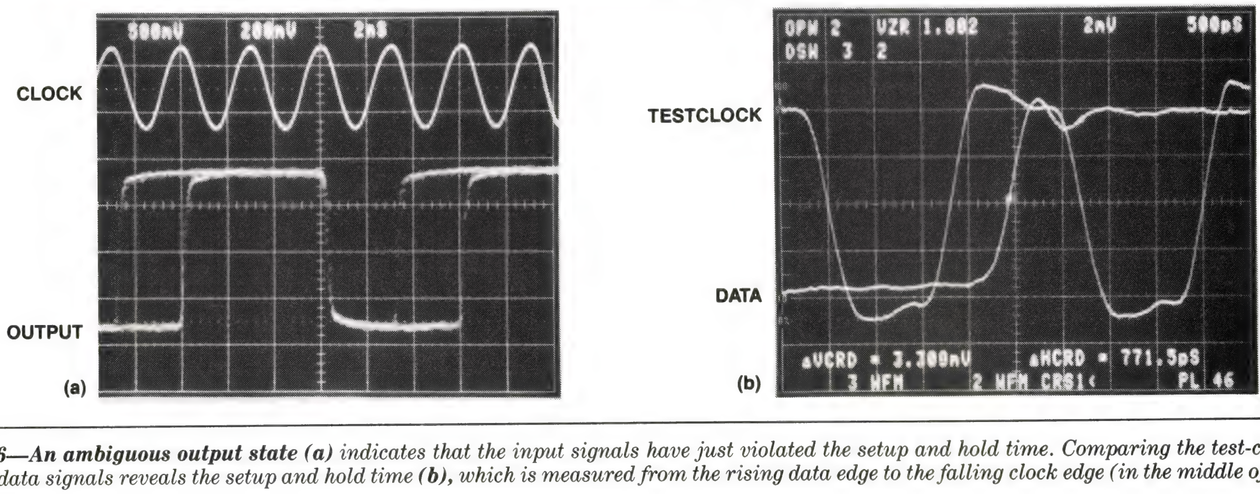


Fig 6—An ambiguous output state (a) *indicates that the input signals have just violated the setup and hold time. Comparing the test-clock and data signals reveals the setup and hold time* ***(b),*** *which is measured from the rising data edge to the falling clock edge (in the middle of the trace).*

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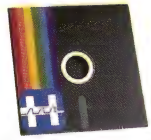

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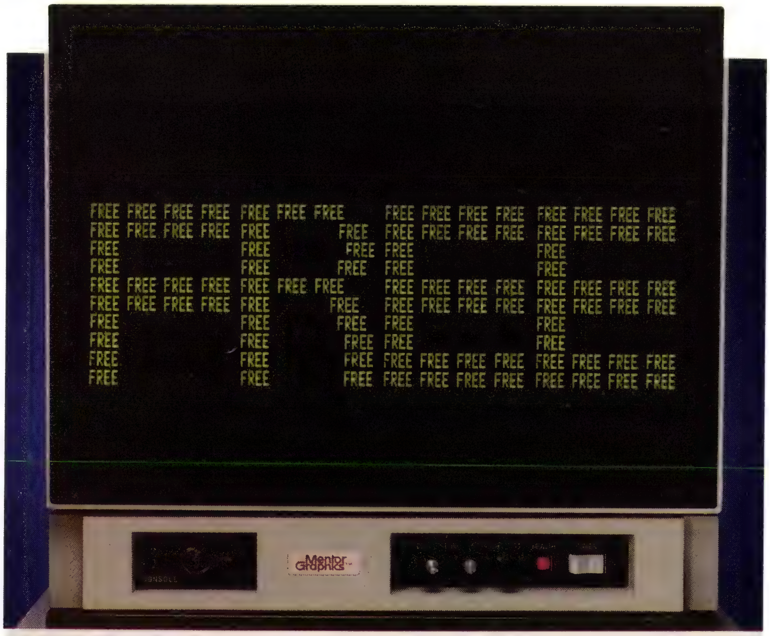

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minus the added input gate delay plus the clock delay. When the setup time equals 250 psec (data equals a high), for example, the hold time equals −300 psec (the setup time for data at a low). The hold time is negative because the flip-flop in the shift register doesn't require that the data be held stable until after the clock transition.

When using a GaAs IC in a circuit design, you have to satisfy both setup and hold time requirements. In this case, the setup time of 250 psec has to be met before the hold time of −300 nsec. You can't take these setup and hold times and compute a minimum pulse-width valid time. These measurements are for single data transitions or for data pulses wide enough that the IC achieves steady-state operation between signal edges.

The Spice prediction for setup time (according to the Q-Chip's data sheet) is about 200 psec. This value is close to the average measured setup time of about 250 psec. The Spice model doesn't include complete parasitic capacitance, which could account for some of the difference between the actual and simulated values.

Two of the entries in **Table 5** appear as waveforms in **Fig 6.** The first **(Fig 6a)** shows the setup-time measurement for the rotate-right input **(Fig 3c).** The clock frequency is 330 MHz; the output shown is an example of the transitional state. This transitional state indicates that the delay between the data and clock inputs violates the shift register's setup time for data=high or its hold time for data=low.

Fig 6b is an example of an actual measurement of data=high setup time (and data=low hold time). The test-clock frequency is 371 MHz, and the rising edge of the data signal precedes the falling edge of the clock signal by 771 psec. This value represents the setup time for data=high and the hold time for data=low. This 771-psec value is one value contributing to the 702-psec average in **Table 5** for the rotate-right setup values (data=high). Similarly, **Fig 7** shows the waveforms for the same input with a data high-to-low transition. The 810-psec value contributes to the 844-psec value listed in **Table 5.**

Measurements represent examples

To verify that your data is statistically correct, you must quantify the bit error rate (BER) of the output signal at the time of the measurement. You can use a BER meter or other event counter to monitor the output signal and to determine when setup or hold has been met to a specified BER. Otherwise, you can consider your results only approximate.

You have to be careful about using the algebraic sum of the setup and hold times to calculate a device's data-valid time—the minimum pulse width that it can capture. This approach is tempting with GaAs devices because of the forbidding difficulties of generating a pulse narrow enough to adequately test for this condition. Nonetheless, testing with a single pulse is the only way to accurately determine the minimum pulse width because the energy associated with the waveform becomes critical to how fast the device switches.

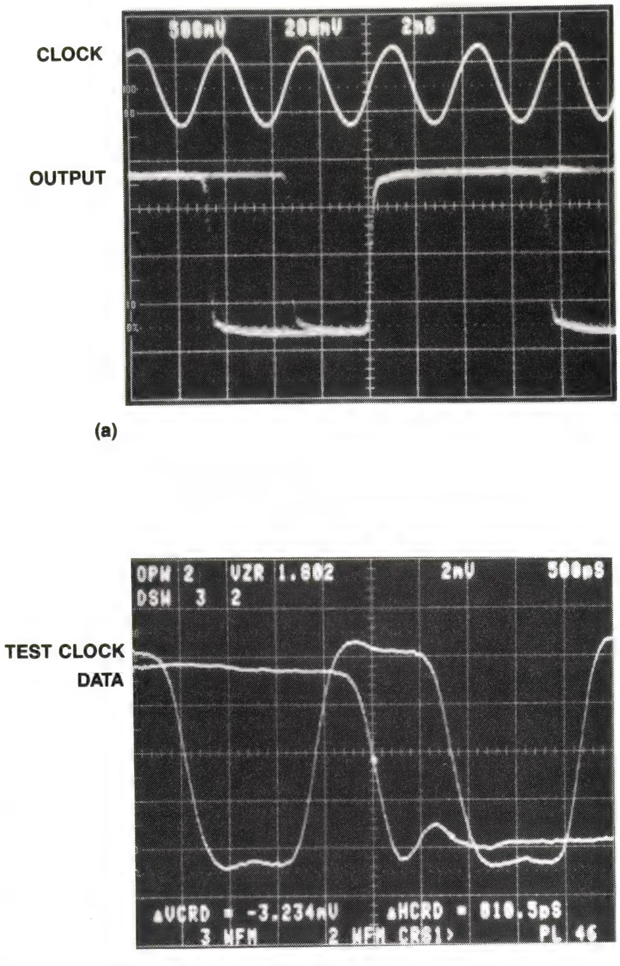

Fig 7—When the output state appears ambiguous (a), the 810-psec interval between the falling data transition and the falling clock edge indicates the setup and hold time (b).

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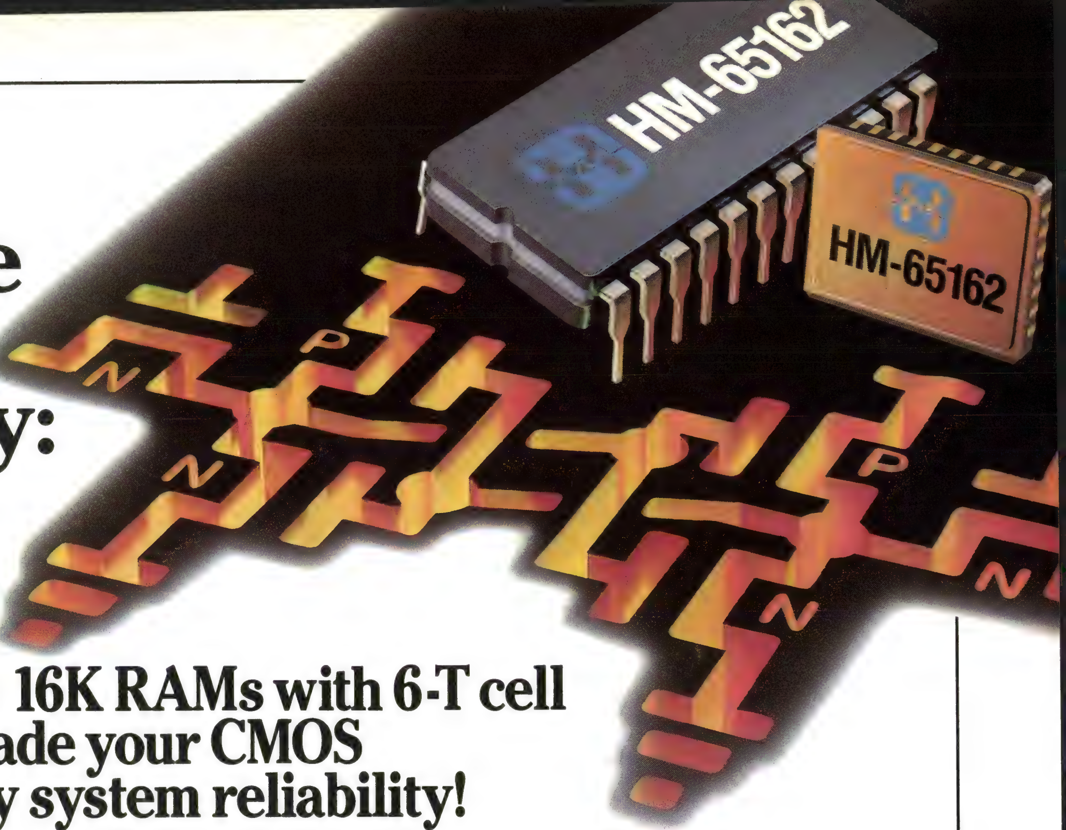

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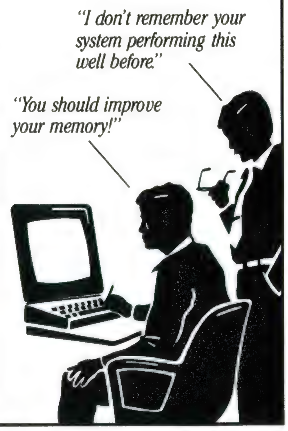
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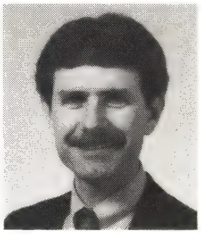
In fact, Spice models show that setup and hold times depend on the test pulse's width until the pulse is sufficiently wide with respect to the clock rate. It's safe to say that the pulse widths used here are sufficiently wide. When working with a pulse wider than about 250 psec, the symmetrical relationship between data=high setup time and data=low hold times is valid. But for shorter pulses, these values are no longer identical. **EDN**

Authors' biographies



Louis Pengue Jr is a senior design engineer with TriQuint Semiconductor (Beaverton, OR), where he performs project management for the Q-Chip semicustom gate array. He originally developed silicon ICs for Tektronix, and afterwards designed GaAs ICs for that company until it formed TriQuint. Louis holds BSIM, BSEE, and MSEE degrees from the Georgia Institute of Technology. His spare time activities include bicycling, skiing, and playing the piano.

Eldon Walters is the marketing product line manager for Tektronix's Lab Instruments Div (Beaverton, OR) where he handles the 7000 Series oscilloscope sampling products. A Tektronix veteran of 13 years, he holds a BS in Economics & Business from Portland State University.

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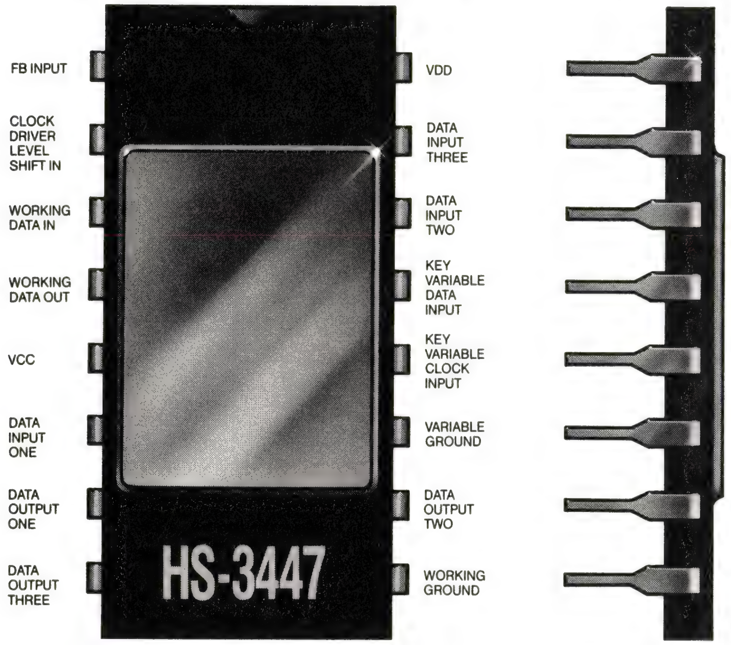

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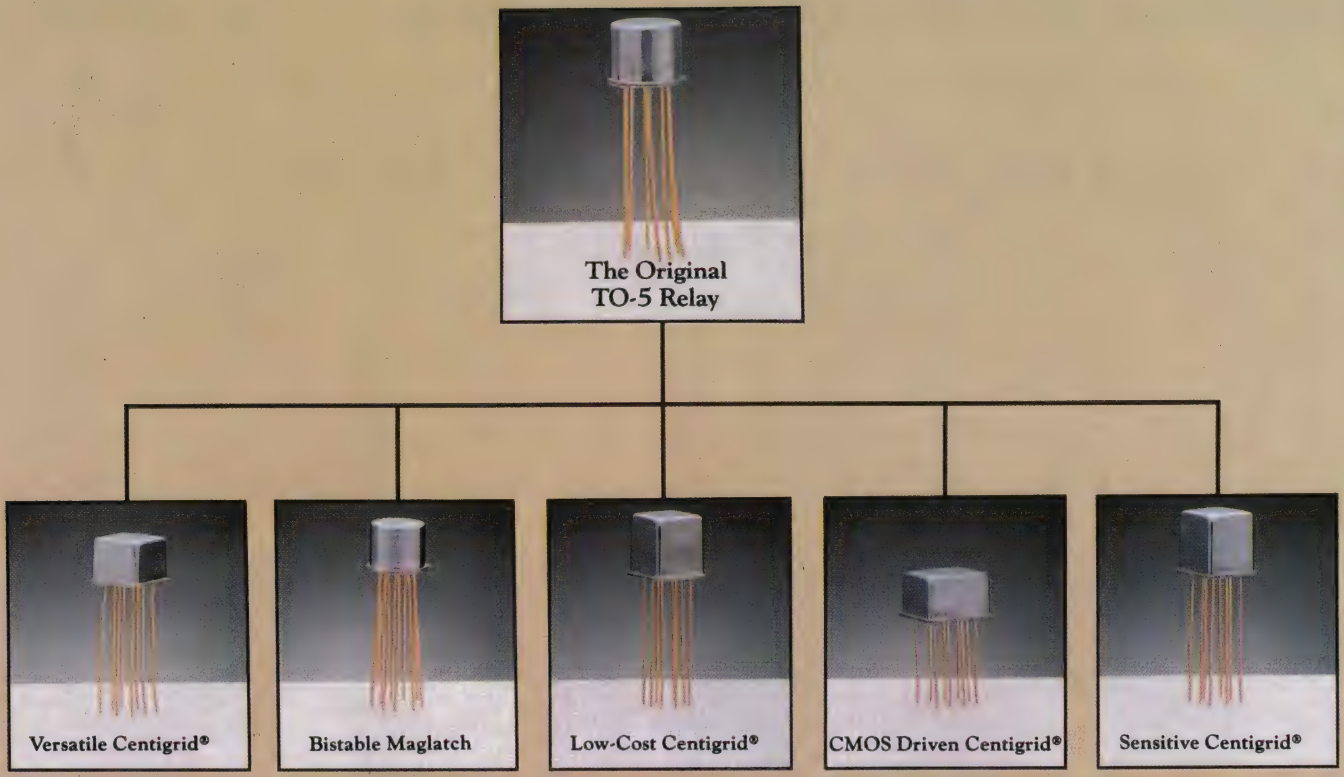

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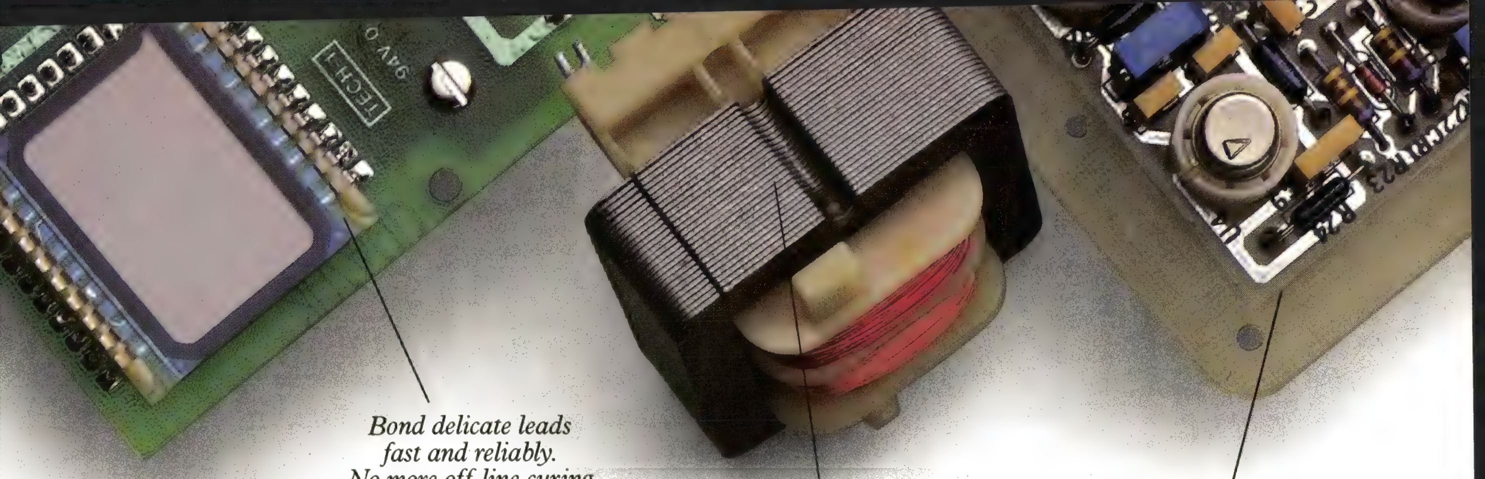

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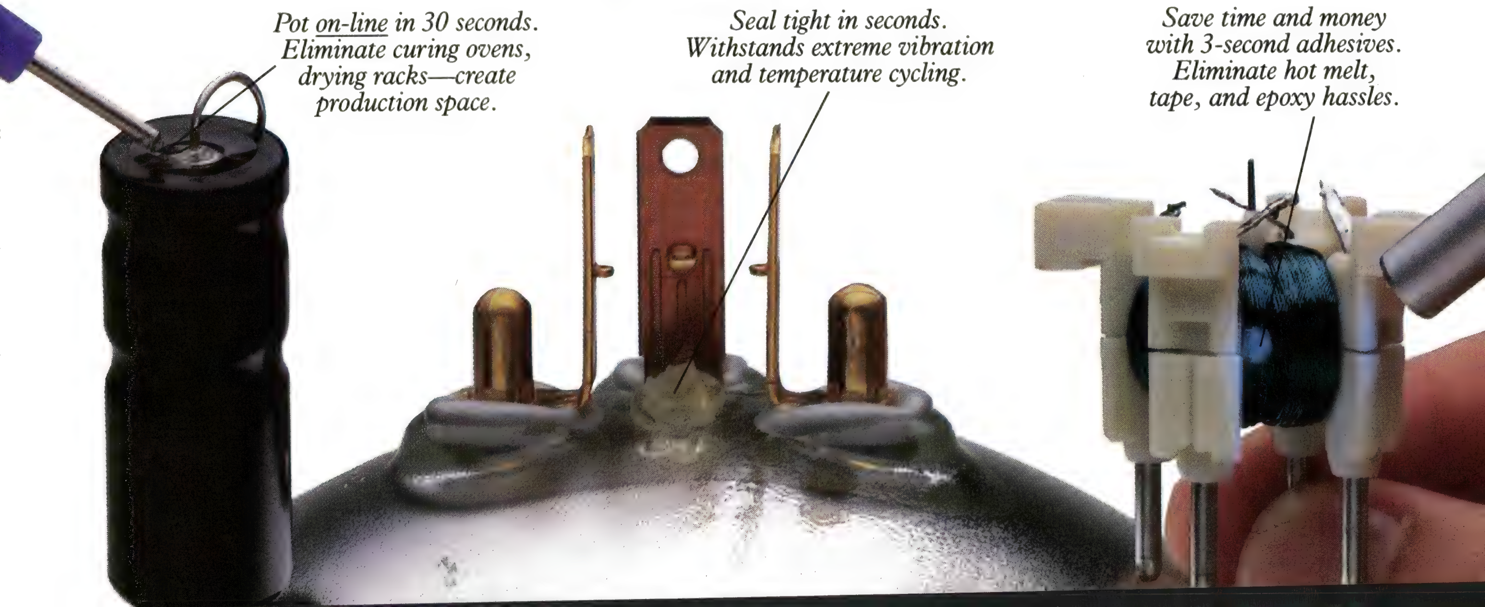

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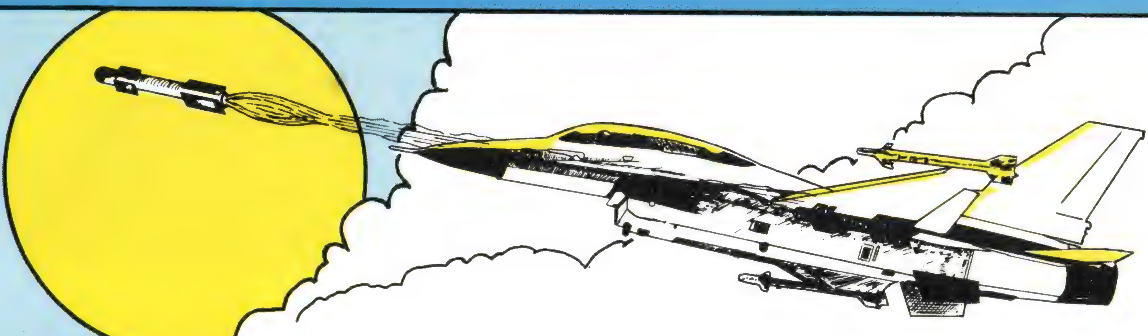

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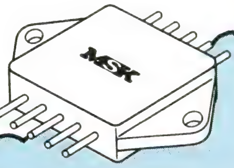

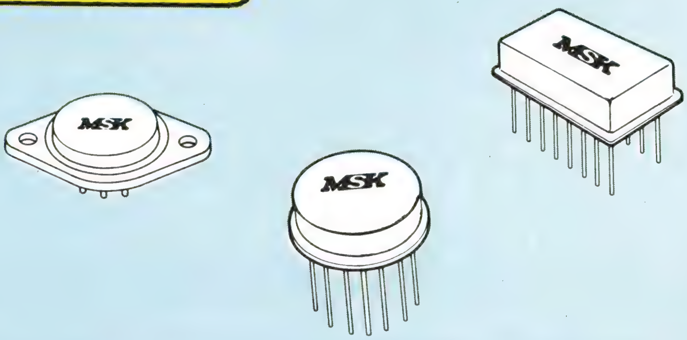

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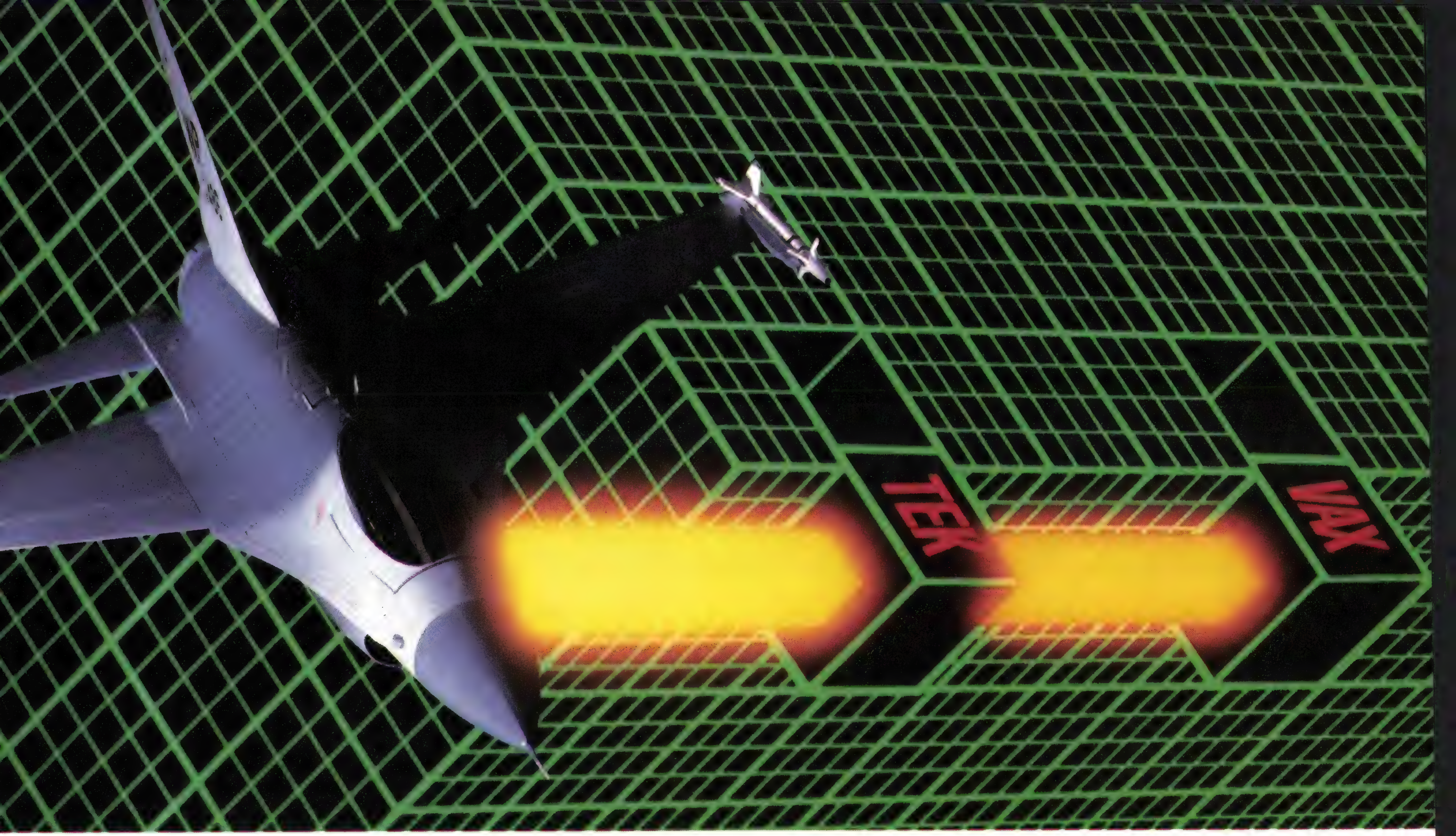

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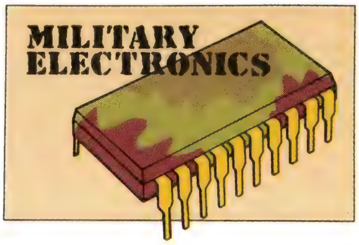


Design low-power, rad-hardened satellite systems

Satellite systems have two major design requirements: They must be radiation hardened, and they must operate on low power. To design such systems, you must use careful shielding, grounding, and decoupling techniques, and you must incorporate low-power, rad-hardened devices, such as rad-hardened CMOS circuits, in your systems.

Bob Pearson, *Harris Semiconductor*

The harsh radiation in space and the limited power available for satellite-carried equipment make radiation hardness and low power consumption prime design goals for space-borne electronic systems. To design a low-power system that also has high resistance to radiation effects—for example, a military weapons system; a scientific space probe; or communications, mapping, reconnaissance, or weather satellites—you can use radiation-hardened CMOS circuits. The rad-hardened CMOS version of the 8086 μP, the 80C86RH (**Fig 1**), for instance, provides a total-dose hardness level as great as 1M rad and consumes only 0.05W/MHz typ.

Simply using radiation-hardened components doesn't automatically guarantee success in designing a radiation-hardened system, however. You must also use proper shielding, grounding, and decoupling techniques. Furthermore, the design must include error-correction schemes, because effecting repairs to systems in Earth's orbit is no small matter. You must also provide for radiation-circumvention procedures that can protect satellite systems during periods of high radiation. (Such circumvention procedures include an orderly shutdown and restart of radiation-sensitive circuits.)

At any rate, if you consider the effects of radiation on your system only after you've completed the initial design, the system is likely to require a costly and time-consuming redesign. To complete a successful design for a space-bound system, you must design your system for radiation hardness from the very beginning of a project.

Particles damage circuits

To ensure that the system you design will be radiation hardened, you must understand the nature of the radiation the circuits and systems may face. For example, the system must be able to withstand the normal radiation in space, which comes primarily from high-energy cosmic particles and from electrons that are traveling in the Earth's magnetic field. The particles and electrons induce ionizing radiation and single-event upsets in a circuit.

A single-event upset occurs when a high-energy particle imparts sufficient energy to a bistable circuit to

Before choosing a radiation-hardened technology, you must understand the types of radiation your system may face.

change its state. To harden their semiconductor devices against the cumulative effects of ionizing doses, semiconductor manufacturers use oxides that are hardened against radiation effects. Such hardened oxides prevent unwanted charges from turning transistor devices on. Likewise, manufacturers place resistors in the feedback paths of cross-coupled bistable circuit elements to dissipate the energy imparted by high-energy particle radiation and prevent an unwanted change of state.

Ionizing and particle radiation primarily cause functional and parametric failures in semiconductor devices. Functional failure is simply the failure to operate properly. Parametric failures occur when a device no longer meets its data-sheet specifications, although it may continue to function properly.

Protect systems from X-rays

Other kinds of radiation can also cause system failures. The radiation from a nuclear explosion in space, for example, would consist primarily of X-rays traveling virtually unattenuated through space. Such X-rays would cause system-generated electromagnetic pulses (SGEMPs) in the system's cables and transmission lines. For the most part, SGEMPs cause failures by fusing metallization lines in unprotected semiconductor devices. Because it's difficult to harden low-power ICs against SGEMP effects, you need to consider the problem at the system level. Using good shielding, grounding, and decoupling techniques will make electronic systems resistant to SGEMP effects.

The semiconductors you incorporate in your system also need to be resistant to such radiation. When X-rays or gamma rays strike p-n semiconductor junctions, the radiation generates charge carriers. For very high dose rates, such as 1×10^{12} rads(Si)/sec, the radiation generates many charge carriers in a very short time. The charge carriers induce photocurrents in the semiconductor material that upset, latch up, and burn out the circuits. To harden their semiconductors against transient dose rates, manufacturers reduce p-n semi-

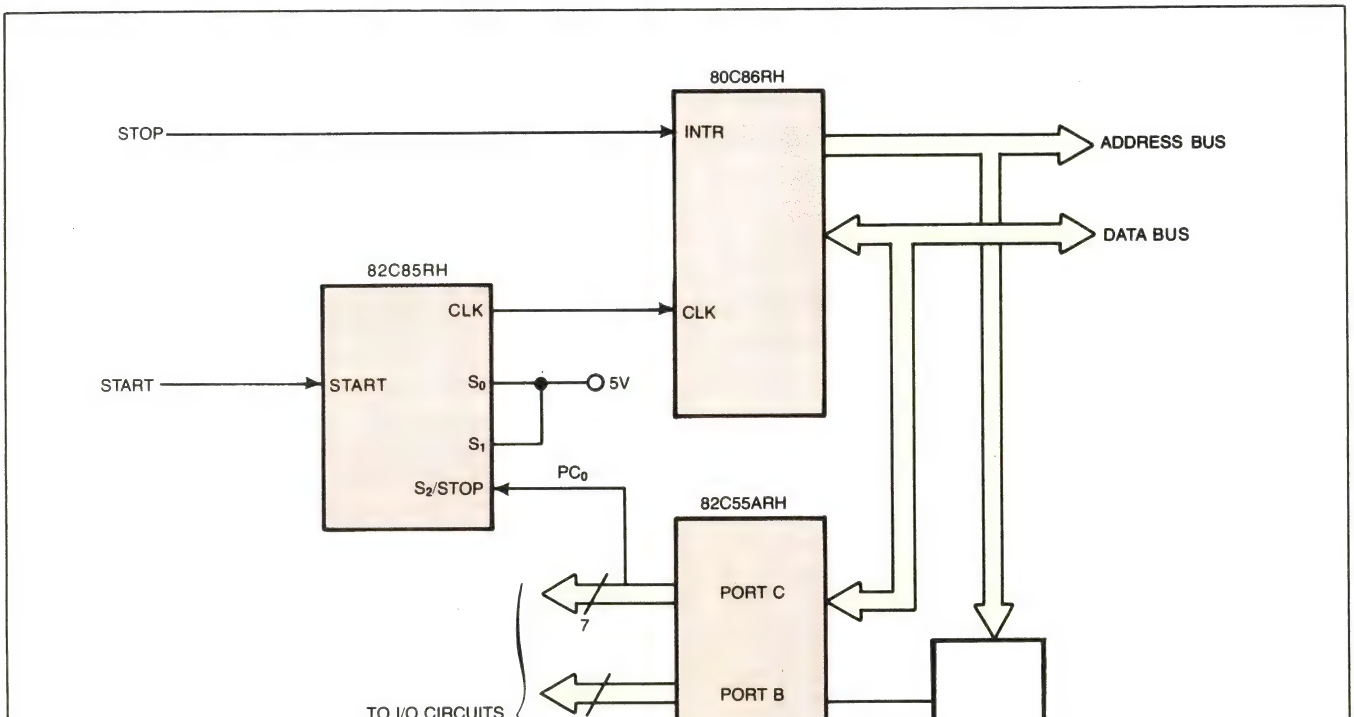


Fig 1—To keep the 80C86RH μP's power consumption to a minimum, *you can use the 82C55ARH programmable-peripheral-interface chip to stop the 82C85RH's internal oscillator circuit. Stopping the oscillator forces the 80C86RH chip into a low-power mode.*

The 80C86RH μP chip

The 80C86RH radiation-hardened 16-bit CMOS μP from Harris Semiconductor (Melbourne, FL) is fabricated in a hardened-field, self-aligned silicon-gate process, a process that involves using oxide layers that are immune to radiation-induced charge buildup. The 80C86RH CPU requires one 5V power supply, and the chip operates at clock frequencies that range from dc to 5 MHz. Standby current is 500 μA, and operating current is 10 mA/MHz.

Even after it receives a total-dose exposure of 100k rad(Si), the 80C86RH will meet its data-sheet specifications. Also, the chip remains free of upsets at radiation levels as high as 1×10^8 rad(Si)/sec. Because it's fabricated as a CMOS device on an epitaxial substrate, the chip isn't subject to latchup conditions. And because it's a CMOS device, the μP chip tolerates exposure to neutron radiation. The manufacturer supplies the μP in a 40-lead brazed-seal ceramic DIP. The chip operates over the full military temperature range.

The 80C86RH μP chip doesn't consume the high power used by CMOS circuits that have floating inputs and thus need external pullup resistors on their I/O signal lines. The 80C86RH provides bus-hold circuits that supply valid logic-level voltages to its internal circuits when external bus drivers are in a high-impedance state.

Because the bus-hold circuits provide current on the μP chip's I/O lines, external devices must overdrive the bus-hold circuit when they transfer data to or from the chip. Thus, bus drivers must supply a minimum 400 μA of sink or source current at valid logic-level voltages to overcome the bus-hold signals and transfer data.

conductor junction volumes so that X-rays and gamma rays generate very small photocurrents within the semiconductors. The most common methods of reducing p-n junction volumes involve using dielectric-isolation (DI) and silicon-on-insulator (SOI) technologies for IC fabrication.

High-energy neutrons from nuclear explosions are another type of radiation that damages semiconductors. The primary damage that neutrons cause is the displacement of silicon atoms from their normal lattice positions within a silicon crystal. The displaced atoms form defect clusters, which degrade bipolar-transistor gain. CMOS devices, however, are relatively immune to the effects of neutron radiation.

Select certified rad-hard parts

Once you understand the effect of radiation on semiconductor devices, you can choose semiconductors that meet your system's survival requirements. Manufacturers of hardened semiconductor devices must guarantee their products' hardness levels. A Radiation Certificate of Compliance comes with each shipment of components. The usual factory-screening method employs a cobalt-60 gamma-cell facility that irradiates sample components. However, different manufacturers may define radiation failures differently. Some may give test results in terms of parametric failures; others may report only functional failures. Functional failures occur at higher dose rates than do parametric failures, however, so be sure to ask manufacturers which type of failure they report.

The final step in the design process is performing your own radiation testing, from the component level to the system level. To test components to specific levels of radiation hardness, you must use standard radiation-screening procedures. Because such radiation testing is destructive, you need to use a statistical-sampling plan instead of testing all of the devices.

To perform the testing, you insert a representative sample of parts into a cobalt-60 gamma cell and irradiate the parts at a high dose rate until the parts have sustained the desired dose. Immediately following irradiation, you test the samples. Note that negligible annealing, or healing, of radiation damage to the parts occurs at room temperature in a short time. Therefore, although very low dose rates over a long time provide the same amount of radiation as does a high dose rate administered over a short period, the parts irradiated over a long period may appear to have sustained less damage than those irradiated over a short period, *High-energy cosmic particles and electrons cause both ionizing-radiation failures and single-event-upset failures.*

because the longer test periods allow annealing time for the parts.

Bias conditions also affect the amount of radiation damage the parts suffer. In post-irradiation testing, parts that are unbiased during irradiation show a better tolerance to gamma radiation than do parts that are biased during irradiation.

For your test results to be meaningful, then, you must know the radiation level of the test, how long the test lasted, whether any delay ensued between the irradiation and testing procedures, and whether the semiconductors were biased during irradiation.

Satellites demand low power

Besides surviving the various effects of radiation, space-borne electronic systems must also operate at low power levels. Solar cells provide the main source of power for satellite equipment, but the limited space available in launch vehicles limits the size of such photovoltaic arrays. The power available for satellite systems, therefore, is limited to a few kilowatts. Further, satellite systems must include batteries—which add weight—so they can operate when the satellite is in the Earth's shadow.

Because power is at such a premium aboard space-borne instruments, it's best to use circuits that you can turn on and off as necessary without affecting the performance of the rest of the system. Such power strobing not only saves power, but increases a component's life, because radiation effects are minimized when a device is unpowered, or unbiased. Likewise, you may be able to save power by running equipment, particularly CMOS circuits, at reduced clock rates or by stopping the clock altogether.

For example, although the radiation-hardened CMOS version of the 8086 μP chip, the 80C86RH, consumes very little power (0.05W/MHz typ), you can reduce power consumption further by turning off the clock signal that controls the chip. Data is not lost when you stop the clock, because the 80C86RH operates in a static mode. The μP's companion chip, the 82C85RH clock generator, lets you control the computer system's clock signals **(Fig 1).** The clock chip supports four modes: the full-speed, slow-speed, stop-clock, and stop-oscillator modes, as **Table 1** shows.

Of these modes, the fast-clock full-speed mode provides for the fastest system response, but it requires the most power. On the other hand, the stop-oscillator mode requires the least power, but it provides for the slowest system response. To decide which type of operation best suits your application, you must carefully weigh your system's response-time and power-consumption requirements.

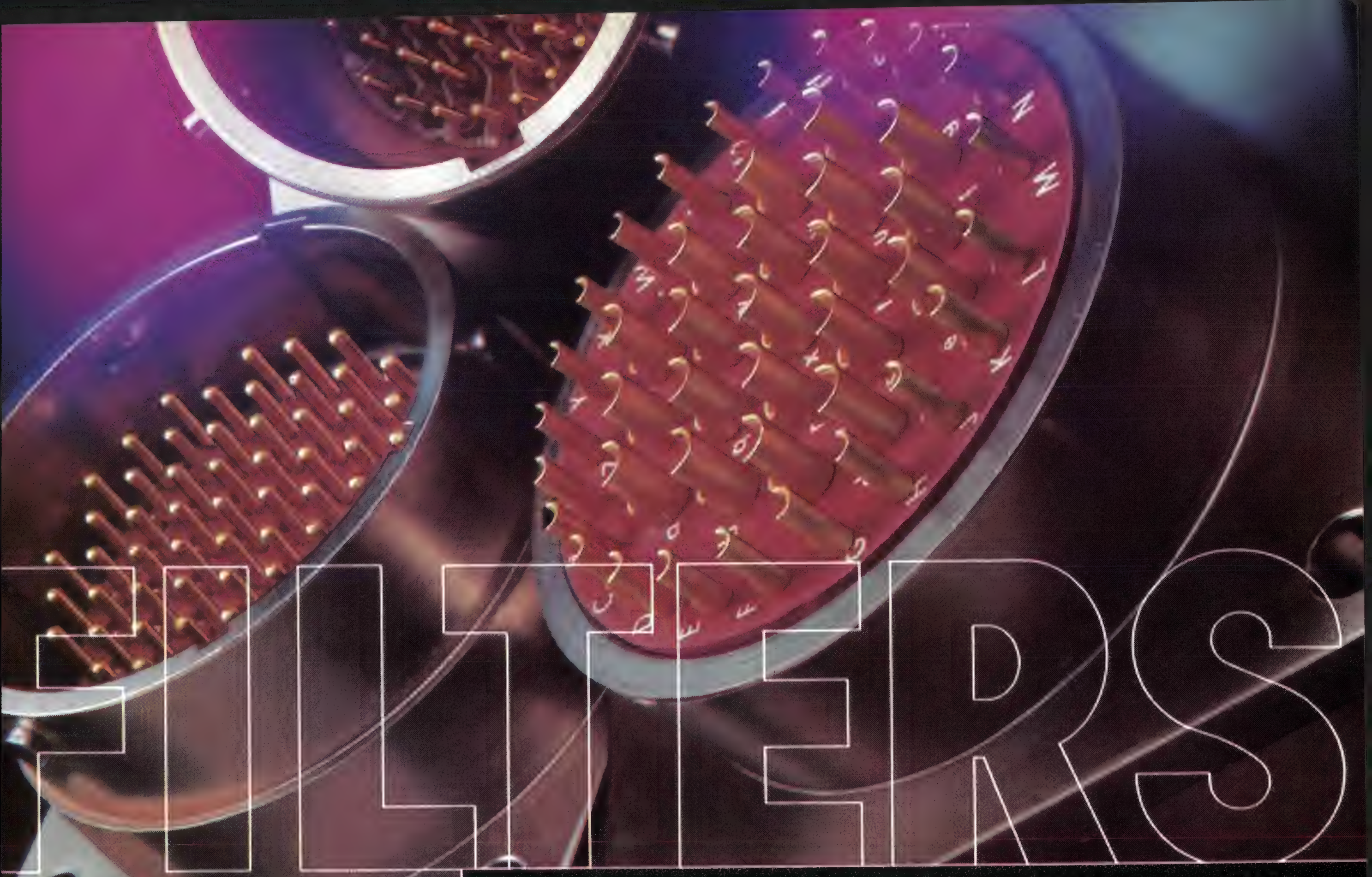
Stop the clock to save power

For example, an Earth-orbit satellite that monitors sunspot activity doesn't require all of its systems to be operating at all times. When the satellite is in the Earth's shadow, there's no need for all of the monitoring instruments to run. To reduce power consumption, then, you can use the 82C85RH chip to shut off the system clock, thus stopping the 80C86RH CPU chip.

To control the CPU and clock circuit, the computer system requires a sensor that can interrupt the CPU when the satellite enters the Earth's shadow. The CPU's interrupt-service subroutine shuts down periph-

TABLE 1—RESPONSE OF A SYSTEM THAT USES AN 82C85RH CLOCK GENERATOR

OPERATING MODE	DESCRIPTION	POWER	PERFORMANCE
STOP OSCILLATOR	ALL SYSTEM CLOCKS AND MAIN CLOCK OSCILLATOR STOP.	MAXIMUM SAVING	SLOWEST RESPONSE (CAUSED BY OSCILLATOR RESTART TIME)
STOP CLOCK	SYSTEM CPU AND PERIPHERAL CLOCKS STOP BUT MAIN CLOCK OSCILLATOR CONTINUES TO RUN AT RATED FREQUENCY.	REDUCED SYSTEM POWER	FAST RESTART. NO OSCILLATOR RESTART TIME.
SLOW	SYSTEM CPU CLOCKS RUN 250 TIMES SLOWER THAN PERIPHERAL AND MAIN CLOCK OSCILLATOR, WHICH RUN AT RATED FREQUENCY.	POWER DISSIPATION IS SLIGHTLY HIGHER THAN POWER DISSIPATION DURING STOP-CLOCK OPERATION.	CONTINUOUS OPERATION AT LOW SPEED
FAST	ALL CLOCKS AND OSCILLATOR RUN AT RATED FREQUENCY.	HIGHEST POWER	FASTEST RESPONSE. FULL-SPEED OPERATION.



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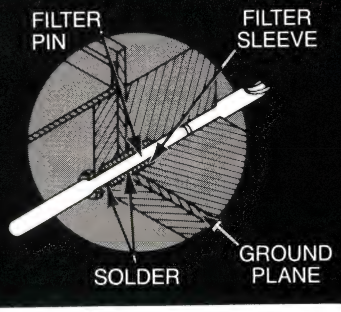

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eral chips and performs other housekeeping tasks. The subroutine also controls an 82C55ARH chip—a hardened programmable-peripheral-interface (PPI) chip—that strobes the clock chip, thus forcing it into the stop-oscillator mode. The stop-oscillator mode turns off both the 82C85RH chip's clock signals and its internal oscillator circuit.

When the 82C85RH chip receives a start pulse from another external sensor, it overrides the stop-oscillator condition and restarts the oscillator circuit. Upon restart, the clock chip doesn't immediately generate a stable clock signal for the 80C86RH μP. Instead, the chip remains idle until it counts 8192 internal clock pulses, after which it passes the clock signal to the μP. The circuit can stabilize during the time between the clock restart and pulse 8192.

Because leaving the stop-oscillator condition causes a delay before the oscillator can become stable, the computer's response to a start signal may not occur in real time. For example, if the oscillator normally operates at 5 MHz, the delay of 8192 clock pulses amounts to a minimum of 1.64 msec between the start pulse and the computer's first operation. For applications that require low power as well as fast response, you can gate the clock off instead of stopping the oscillator. The 82C85RH provides a stop-clock mode that stops the clock signals but lets the oscillator continue running.

EDN

Author's biography

Bob Pearson is a product-marketing manager with Harris Semiconductor's Custom Integrated Circuits Division in Melbourne, FL. He has responsibility for the company's radiation-hardened μP and peripheral products and rad hard CMOS PROMs. Bob received a BSEE from Rutgers University and an MBA from the University of Texas at Dallas. He enjoys scuba diving and water skiing during his leisure time.

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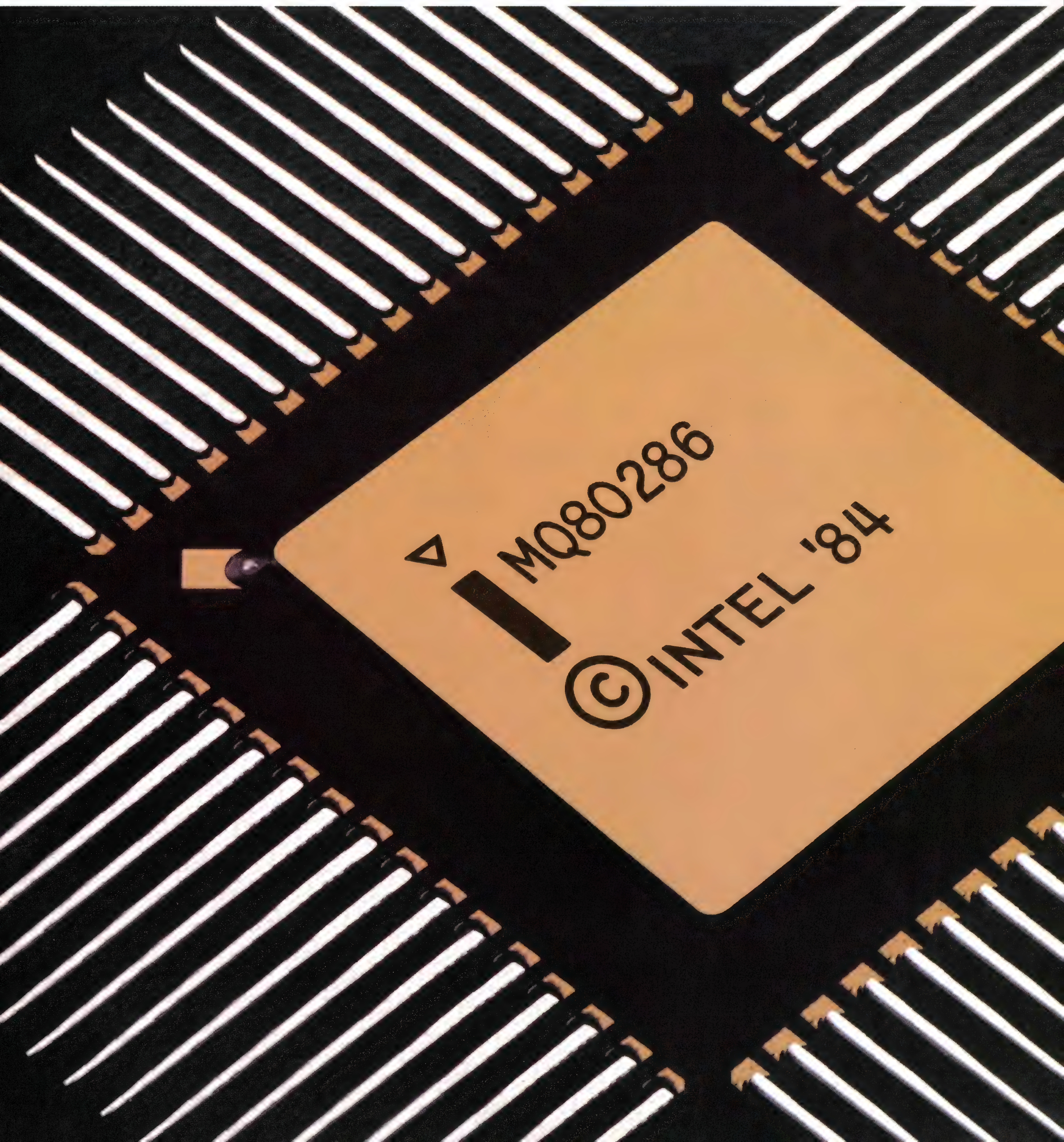

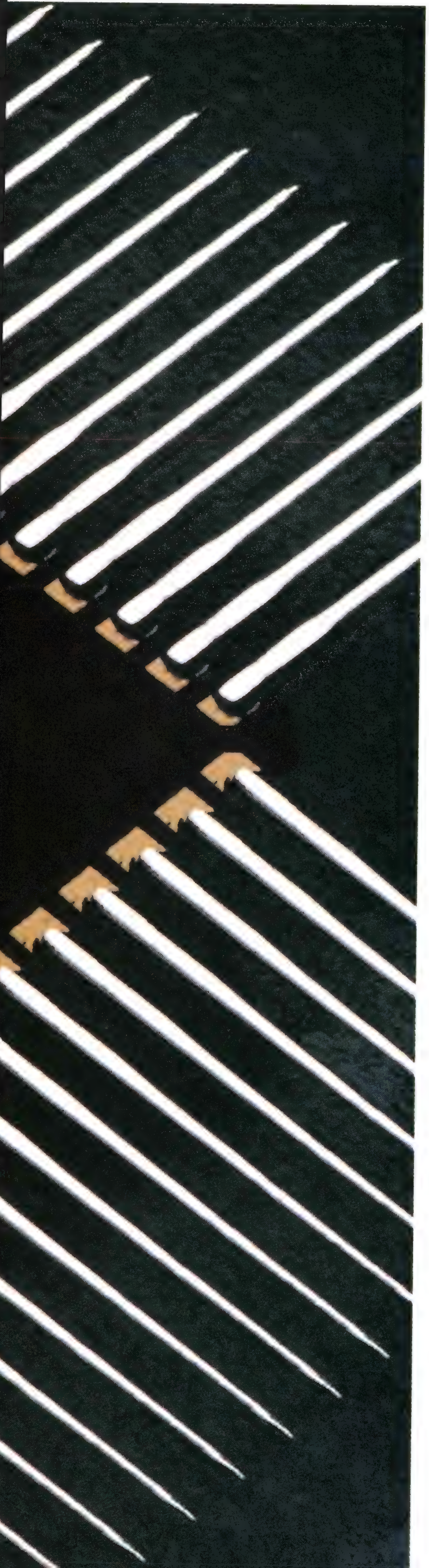

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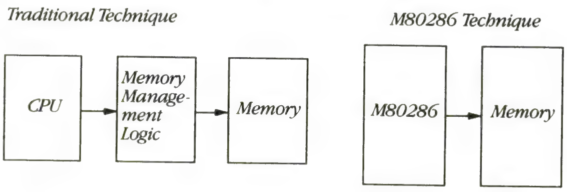

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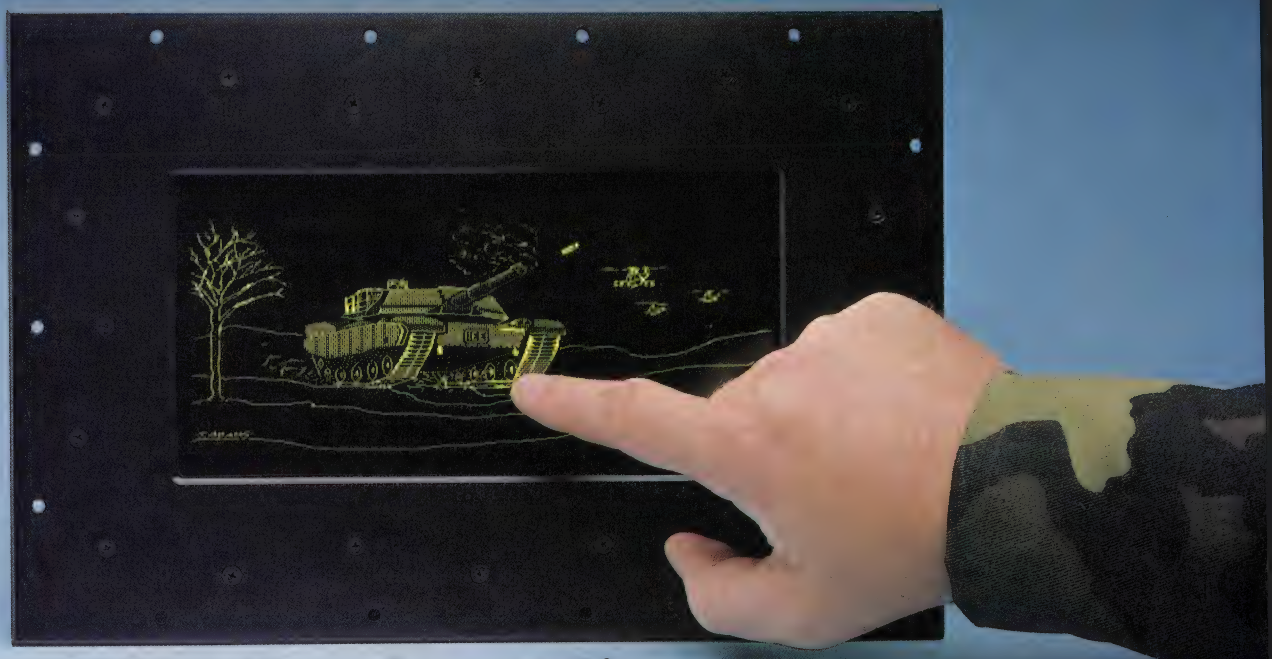

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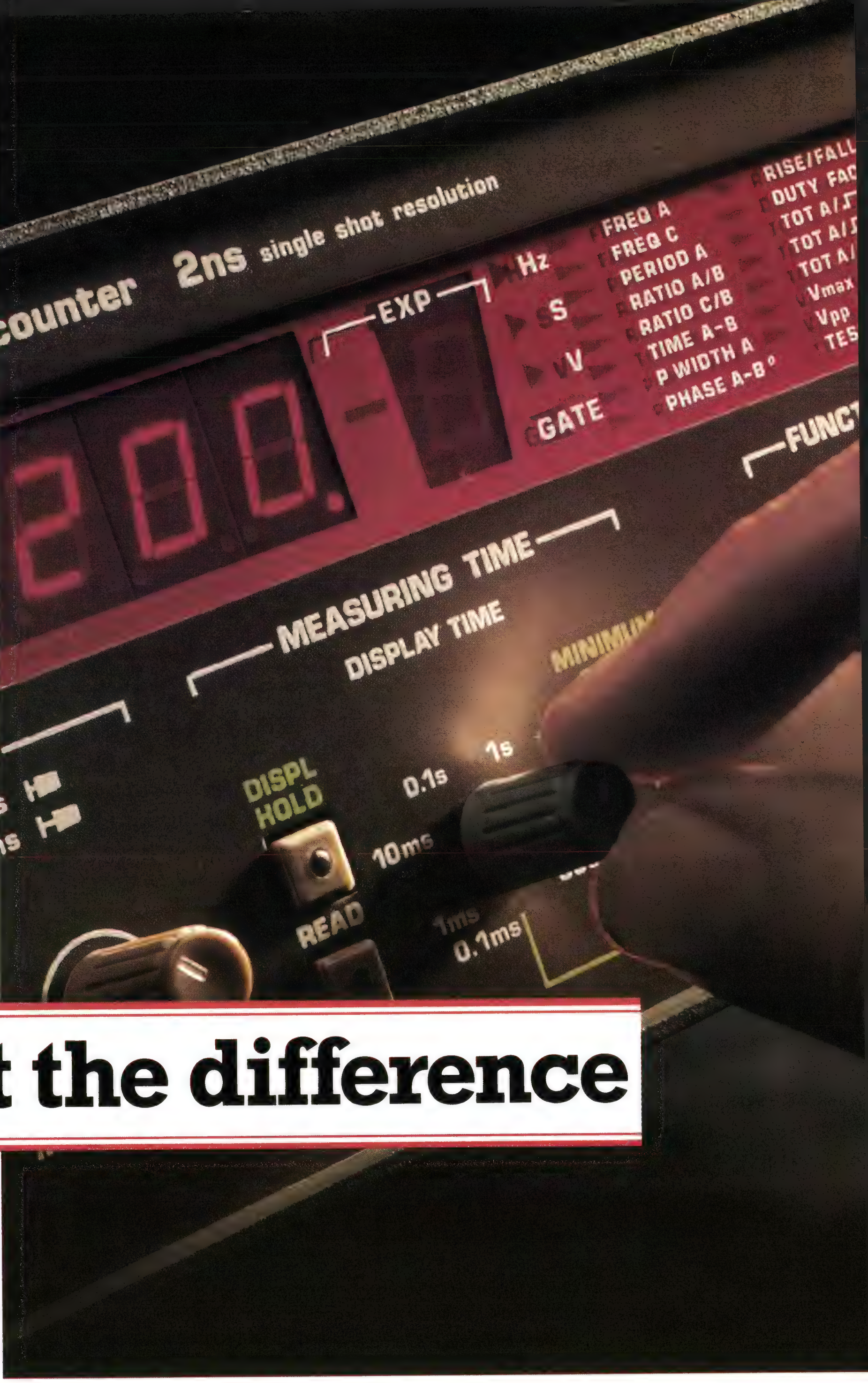

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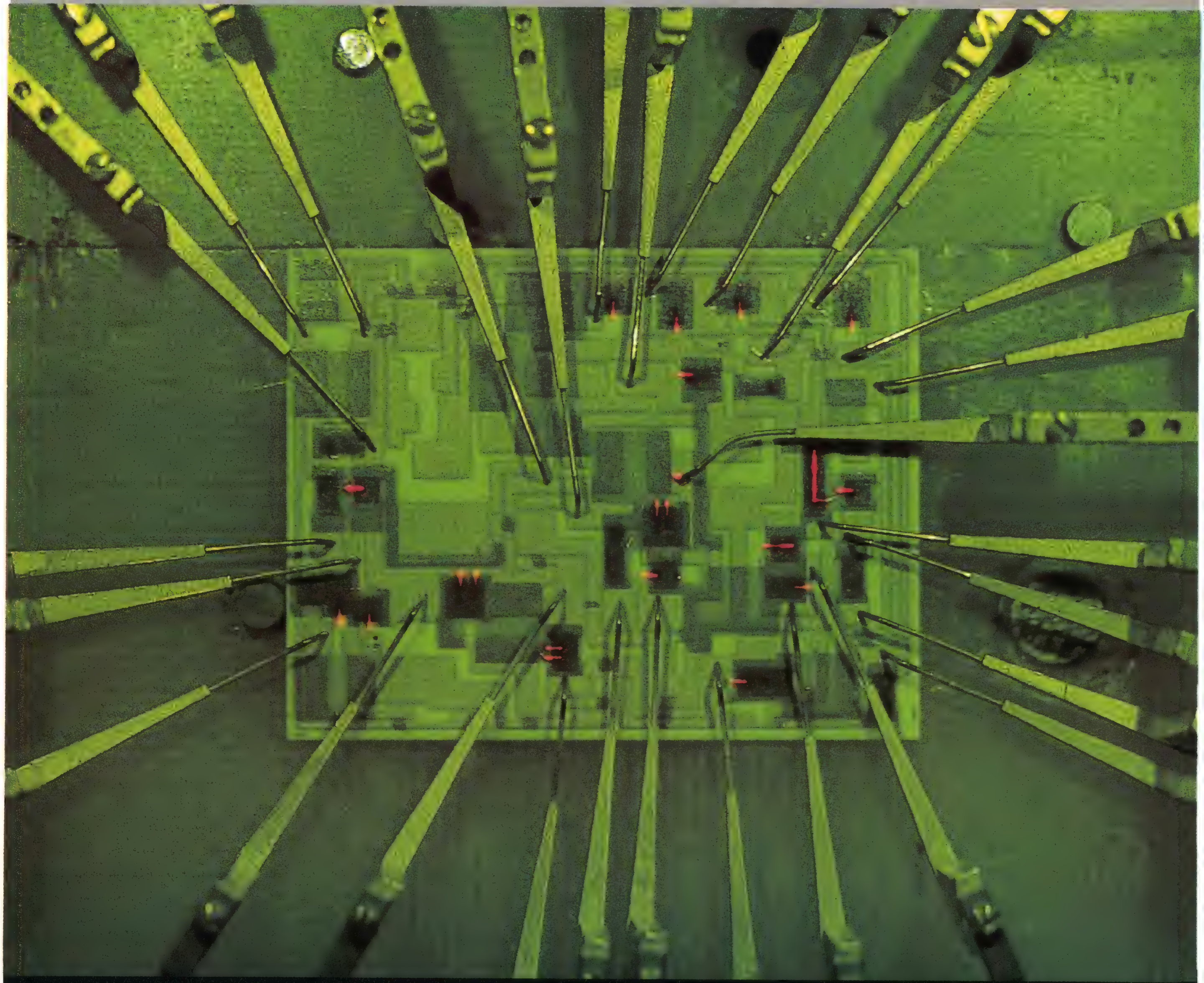

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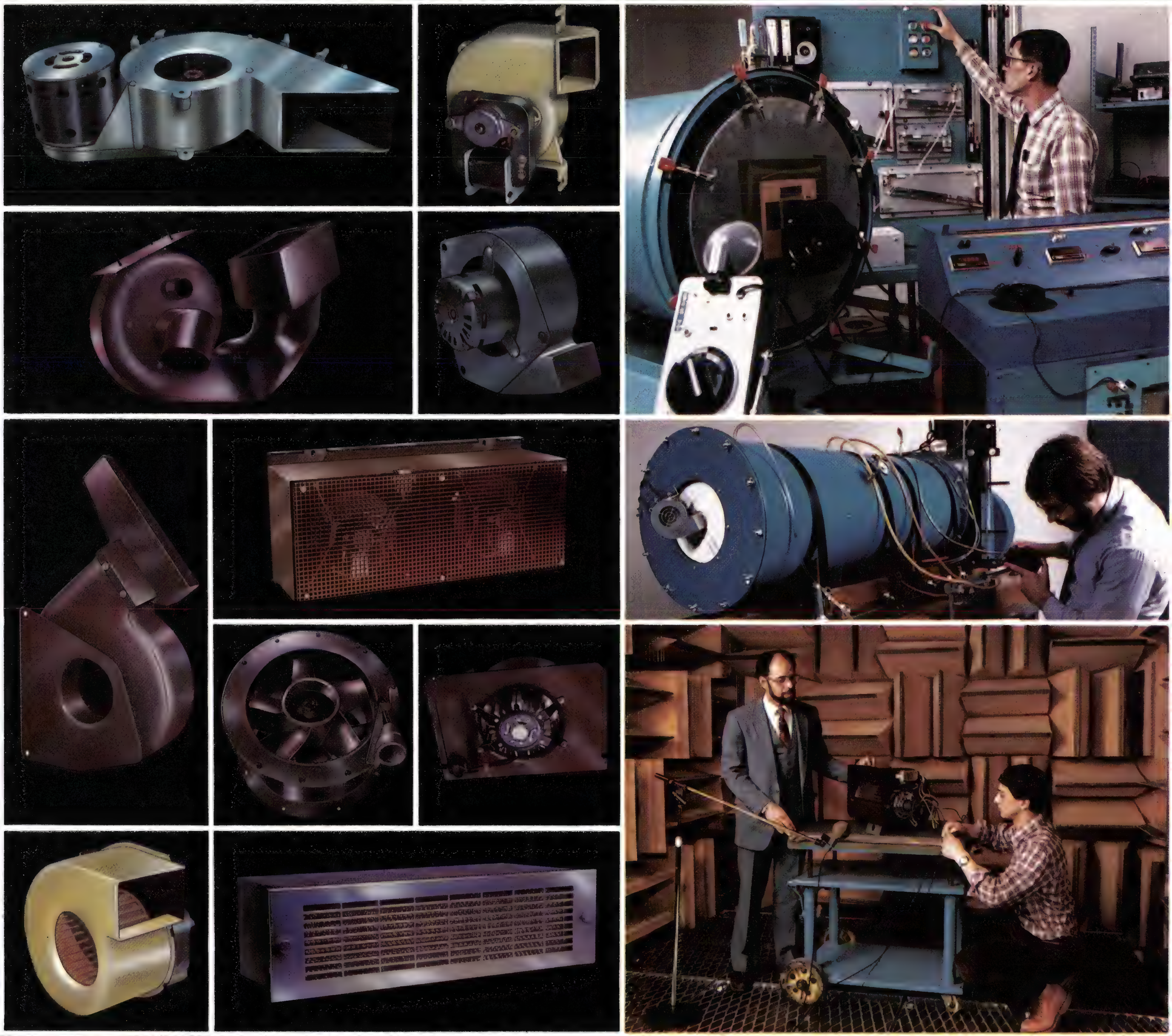

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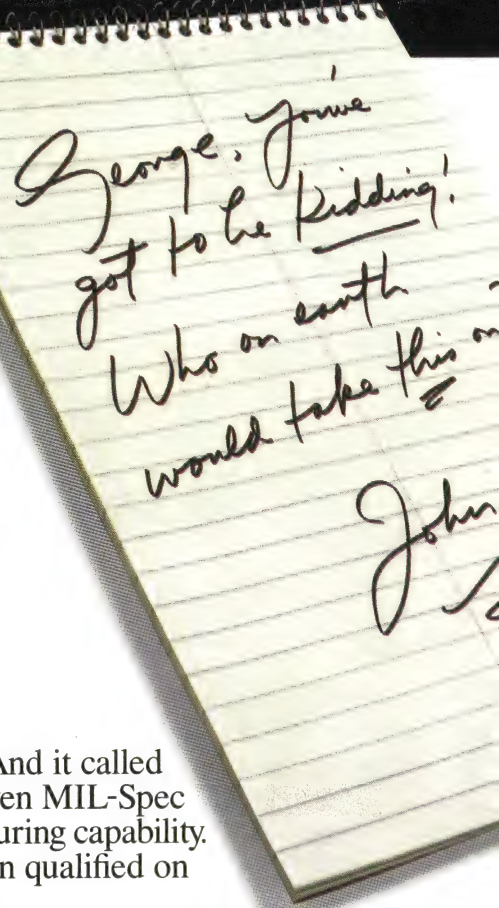

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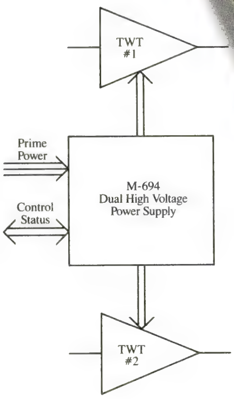

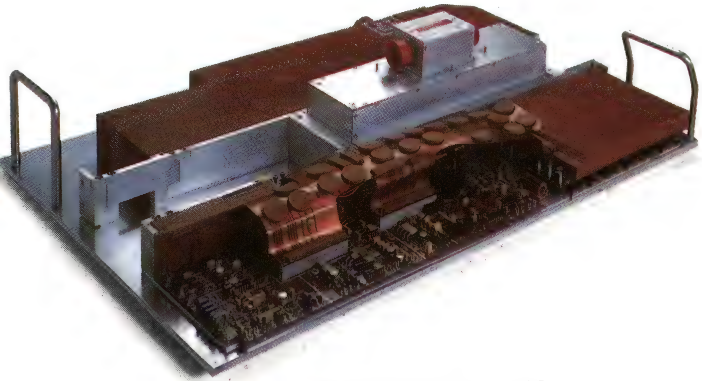

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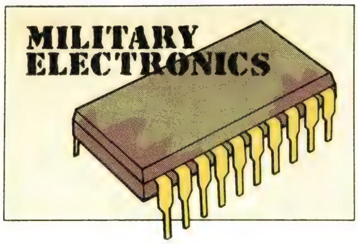

Precision components let you build effective EW radars

To protect radar transmitters from power losses, spurious emissions, and other irregularities that lower performance, use precision transmitter microwave components and careful design techniques.

John McCrea and Charlie Schumann,
Waveline Inc

Radar equipment and its controlling computers are some of the most important elements of an electronic warfare (EW) system. Such a system must not only function under demanding battlefield conditions, but must operate over a frequency range (4.75 to 18 GHz) in which less-than-optimum performance would compromise a mission. Radar transmitters are particularly prone to power losses, spurious emissions, and other irregularities that lower performance. In order to form an effective radar system, therefore, you must use transmitter microwave components (such as waveguides, filters, couplers, switches, and dummy loads) that meet high standards of precision, quality, reliability, and repeatability.

EW radar systems (consisting of transmitters, receivers, and controlling computers) must operate under demanding battlefield conditions. Radar operates at high frequencies (extending into the gigahertz microwave region), where transmission losses can affect system performance and compromise the EW mission. The transmission path in a radar system must exhibit very low losses and low leakage so that only a fraction of the input power is lost within the system.

High-power radar transmitters, which use a traveling-wave tube (TWT), klystron, or other device for the power source, can radiate at a specific frequency or over a range of frequencies. In either case, the radiated signal's output power, stability, and purity are critical characteristics. Signal purity is particularly important, because a microwave transmitter can radiate harmonics that have significant amplitudes. Even a harmonic with a power content only one-thousandth that of the fundamental signal can affect a radar receiver's ability to detect incoming echoes from a target.

Consider a system that's operating on the deck of an aircraft carrier and transmitting signals in the S band. Suppose that the system is also radiating lower-power harmonics in the C and X bands. The amplitude of the harmonics could be high enough to render sensitive radar receivers useless by preventing them from performing their functions in the C and X bands. When the receivers are close to the transmitter, harmonics are even more of a problem. To make the receivers functional, you would have to place a filter at the output of the power source to absorb the harmonics.

Mismatches within the system can also create another problem during signal transmission: reflections. Reflections can return significant amounts of energy to the microwave power source, and they can even destroy it in some cases. In general, reflections reduce system

Radar transmitters are particularly prone to power losses, spurious emissions, and other irregularities that lower performance.

efficiency and increase system losses, setting the stage for premature breakdowns. You can provide some protection against reflections by connecting an isolator between the source and the antenna. The isolator diverts any energy that the antenna doesn't accept to an RF termination (or load), which dissipates the power without reflection.

Spurious emission is yet another transmission problem that can be caused by faulty waveguide components. If you misalign transmission-line elements or any other components, RF energy will leak from the misaligned joint. To eliminate such emissions, you must make sure all interfaces are well matched, and you must use proper gaskets.

In view of the problems that can occur in a radar system's transmission path, designers must take care not to overlook the details of system design. Consider the selection of harmonic filters, for instance. If you

Inside an electronic-warfare radar system

Self-protecting electronic-warfare (EW) radar systems, which are used in air-, sea- and land-based military applications, locate enemy radar signals and radar sites and sense the presence of tracking signals. They can also identify enemy tracking signals, jam enemy radar systems, provide decoys to confuse enemy tracking radars, and confuse guided missiles.

An EW radar system essentially consists of transmitter and receiver sections and a control computer. The system's radar equipment must be able to carry out its own mission without being detected by the enemy's radar equipment. Most radar systems perform four basic activities: searching, tracking, jamming, and guidance. The configuration of such systems varies widely, but a typical battlefield system would include a search transmitter with a tracking or guidance operating mode, a jamming transmitter, and a radar warning receiver. An aircraft or ship may contain search radar to locate enemy vessels, and a radar-jamming system to confuse the enemy's search radar.

The network in **Fig A** is a representative search-radar system for an aircraft or ship. A search-radar system is characterized by high output power but relatively narrow bandwidth. A typical search-radar system would include a high-power RF source (a multicavity klystron, traveling-wave tube, or solid-state amplifier), a harmonic filter, a ferrite circulator, dummy loads, directional couplers, and switches. Waveguide structures serve to interconnect the elements.

Radar-jamming systems **(Fig B)** are significantly different from search-radar systems in that they span a wider bandwidth. The primary function of these systems' transmitters is to generate a strong interference signal in the RF band that the enemy is using for communications, search, or guidance transmissions. A jamming system disrupts communications by increasing noise levels, saturat-

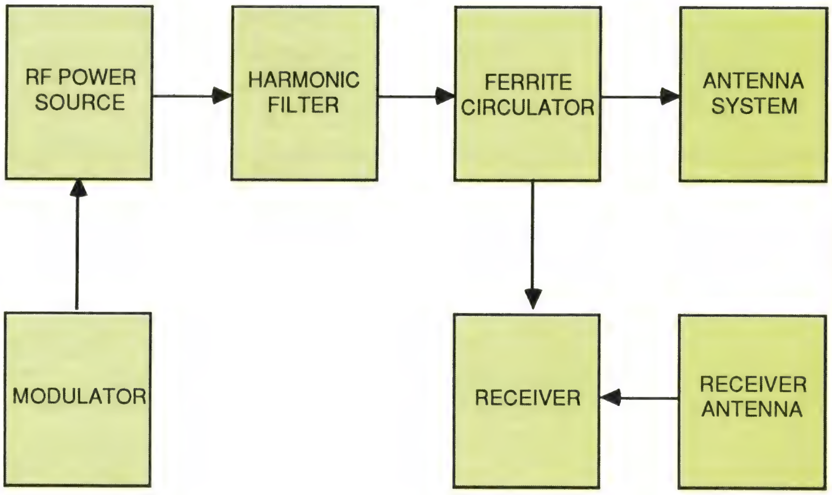

***Fig A—High-power output and narrow bandwidth** characterize a typical search-radar system. Such a system typically includes a high-power RF source, a harmonic filter, a circulator, dummy loads, directional couplers, and switches.*

need harmonic filters, make sure you select units that spec minimum insertion loss at the system's fundamental frequency. Also make sure that you take the high-order modes into account when you look at the filter's harmonic-suppression characteristics. Ferrite circulators (isolators) must also exhibit minimum insertion loss, have the proper voltage standing-wave-ratio (VSWR) characteristics, and be able to accommodate high peak-power levels.

When you configure the transmission path, be sure to use precisely machined components for the entire waveguide run. To reduce insertion losses, use waveguides whose internal surfaces are plated with silver or some other finish. The radar system will probably be operating in an airplane, so the waveguides must be able to withstand pressurization. To prevent deformation of the waveguides in a pressurized environment, you may have to select waveguides that are reinforced

ing the receiver input, or confusing a receiver with deceptive signals. In digital communications, a jamming signal increases the error rate, making communications unreliable. In essence, jamming systems fall into two categories: Some generate noise to prevent information exchanges between enemy installations; others both minimize the enemy's ability to locate aircraft and disrupt the enemy's guided-missile control systems.

Traveling-wave tube (TWT) transmitters are becoming the predominant type of transmitter in radar-jamming systems that operate at microwave frequencies. TWTs generate greater output power and accommodate wider operating bandwidths than do solid-state amplifiers. TWTs are also more suitable for operation at frequencies in excess of 20 GHz—a level that's becoming more common in today's EW radar applications.

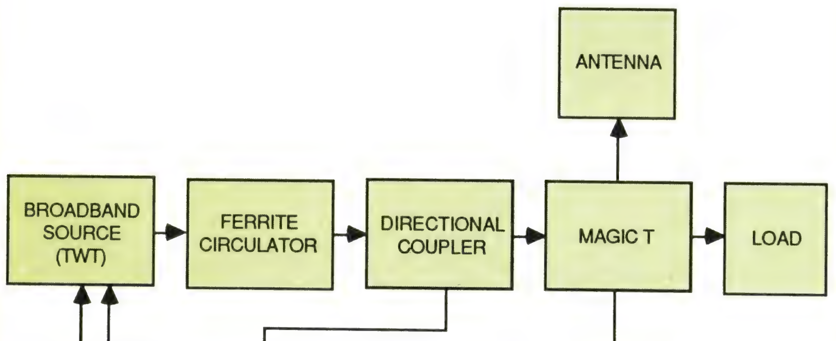

***Fig B—Radar-jamming systems operate over a wider bandwidth** than do search radars. They disrupt communications by increasing noise levels, saturating receiver inputs, or emitting deceptive signals.*

Although EW radar systems employ a variety of receiver designs, aircraft applications commonly employ the radar warning receiver (RWR). The RWR's primary function is to alert the flight crew to potential threats to the aircraft, such as the presence of an RF signal that illuminates the aircraft (an enemy's search radar), or the approach of an enemy missile.

Most RWRs have a direction-finding capability that's available to the pilot on a scope display in the cockpit. This display provides the coordinates of potential threats, so the pilot can take evasive action. Typically, the simple RWRs developed in the 1960s merely indicated the presence of a threat. Today's more sophisticated threat warning systems identify a threat, assess its seriousness and assign it a priority in the event of multiple threats, and determine the proper response. The response can be a simple jamming signal, evasive action, or preparation for combat. In this sense, the threat warning system serves as a resource manager for the aircraft's armament and EW-radar systems.

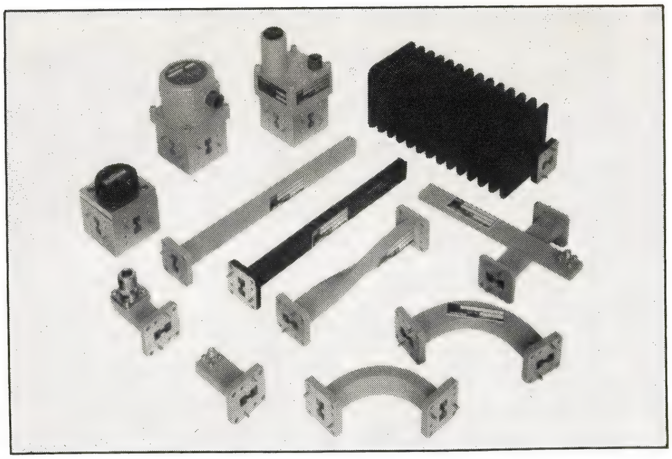

Fig 1—Double-ridged waveguides, *such as those shown, offer the optimum tradeoffs for airborne-radar-system design. For example, double-ridged waveguides have a lower insertion-loss spec than does coaxial cable, and they're smaller and lighter than rectangular guides. Unlike coaxial cable, double-ridged waveguides can accommodate the 150W average and 5-kW peak power typically generated by radar-jamming systems.*

for operation at L- or S-band frequencies.

Furthermore, waveguides are as sensitive to environmental conditions as are any other components, so when you specify waveguide components for radar systems, you must consider the atmospheric conditions and temperature range the systems will be operating in. Because EW radar systems may be exposed to the elements, you must make sure the waveguides you specify will operate in such atmospheric conditions as rain, excessive humidity, ice, and wind.

It's also important to select the right type of waveguide for your application. Radar-jamming systems usually operate in the 4.75- to 18-GHz frequency range. EW-system transmission lines that operate at these frequencies employ double-ridged waveguides **(Fig 1)** instead of the conventional rectangular types. For airborne applications, the ridged waveguide offers system designers the optimum tradeoffs among power-handling capability, bandwidth, insertion loss, size, and weight. For instance, double-ridged waveguides have a lower insertion-loss spec than does coaxial cable, and they're smaller and lighter than rectangular guides. And although ridged waveguides can't match the power-handling capability of rectangular guides, they can handle more power than can coaxial cable. Typically,

TABLE 1—REPRESENTATIVE WAVEGUIDE SPECIFICATIONS FOUND IN MIL HANDBOOK 216*

TYPE DESIGNATION[1]	CUTOFF FOR TE_{10} MODE (GHz)	CUTOFF FOR TE_{20} MODE (GHz)	RECOMMENDED FREQUENCY-RANGE TE_{10} MODE (GHz)	MATERIAL	FLANGE USED WITH		$f=\sqrt{3}f_{c_{10}}$**	
					MIL-F-39000/( )	UG-( )/U	THEORETICAL ATTENUATION[2] (dB/ft)	PEAK POWER RATING[3] (kW)
WRD350D24-	2.915	8.620	3.500 TO 8.200	ALUMINUM ALLOY	3.010	1574	0.0307	151.3
				BRASS	3-011	1575	0.0303	
				COPPER	3-011	1575	0.0204	
				SILVER ALLOY	3-011	1575	0.0218	
WRD475D24-	3.961	11.705	4.750 TO 11.000	ALUMINUM ALLOY	3-013	1577	0.0487	83.72
				BRASS	3-014	1578	0.0481	
				COPPER	3-014	1578	0.0324	
				SILVER ALLOY	3-014	1578	0.0347	
WRD750D24-	6.239	18.464	7.500 TO 18.000	ALUMINUM ALLOY	3-016	1580	0.0964	33.58
				BRASS	3-017	1581	0.0951	
				COPPER	3-017	1581	0.0641	
				SILVER ALLOY	3-017	1581	0.0686	
WRD110C24-	9.363	27.080	11.000 TO 26.500	ALUMINUM ALLOY	3-019	1583	0.171	15.63
				BRASS	3-020	1584	0.169	
				COPPER	3-020	1584	0.114	
				SILVER ALLOY	3-020	1584	0.122	
WRD180C24-	14.995	44.285	18.000 TO 40.000	ALUMINUM ALLOY	3-022	1586	0.358	5.834
				BRASS	3-023	1587	0.353	
				COPPER	3-023	1587	0.238	
				SILVER ALLOY	3-023	1587	0.255	

NOTES:

* FROM TABLE 6.XXVIII, *DOUBLE-RIDGED WAVEGUIDES, BANDWIDTH RATIO 2.4:1 (MIL-W-23351/4).*

** $f_{c_{10}}$ = CUTOFF FREQUENCY FOR TE_{10} MODE.

1. COMPLETE TYPE DESIGNATION WILL INCLUDE AN ADDITIONAL SYMBOL (A, B, C, OR S) TO INDICATE MATERIAL.
2. TYPICAL RESISTIVITIES OF MATERIALS (AT 20°C): ALUMINUM ALLOY (6061) = 4.00 $\mu\Omega$-CM; BRASS = 3.9 $\mu\Omega$-CM; COPPER = 1.77 $\mu\Omega$-CM; SILVER ALLOY (COIN SILVER) = 2.03 $\mu\Omega$-CM
3. BASED ON THE E-FIELD-PRODUCED BREAKDOWN IN A NONPRESSURIZED AIR DIELECTRIC WAVEGUIDE UNDER CONTINUOUS-WAVE (CW) CONDITIONS. THE BREAKDOWN STRENGTH OF AIR WAS CONSIDERED TO BE 15,000 V/CM, CORNER RADII CONSIDERED.

To eliminate leakage of RF energy from misaligned transmission-line elements or other components, make sure all interfaces are well matched.

jamming systems generate average and peak powers of 150W and 5 kW, respectively. Double-ridged waveguides can accommodate these levels; coaxial cable can't.

Furthermore, a single type of double-ridged waveguide will span the same bandwidth as two or more different types of rectangular guides. This capability is very important in radar-jamming systems, because the equipment in such systems must be tunable: That is, it must be capable of sweeping across a range of frequencies to detect the tracking frequency of hostile radars.

Standards for the various EW radar transmission-line media (coax, and rectangular, circular, ridged, and elliptical waveguides) and their support components can be found in MIL Handbook 216. The handbook specifies types of waveguides and their operating modes, operating frequencies, insertion-loss figures, power-handling capabilities, construction materials, and wall finishes. Manufacturers and system designers should conform strictly to the specifications and restrictions listed in the handbook; these specs constitute the accepted standards for the waveguides used in many types of EW radar equipment. Section 6 of the handbook contains specifications and characteristics for double-ridged waveguides **(Table 1).**

TABLE 2—CRITICAL SPECIFICATIONS FOR EW WAVEGUIDES AND SUPPORT COMPONENTS

WAVEGUIDE
- PROPER RANGE OF FREQUENCY AND MODE
- INSERTION LOSS (ATTENUATION/UNIT LENGTH)
- POWER CAPABILITY

MECHANICAL
- FREEDOM FROM DEFORMATION AND/OR CONTAMINATION
- PROPER THICKNESS TO WITHSTAND PRESSURIZATION AND INSTALLATION

CIRCULATORS/ISOLATORS
- ALL THE REQUIREMENTS OF STANDARD WAVEGUIDES PLUS:
- LOW INSERTION LOSS
- HIGH ISOLATION
- LOW VSWR AT THE DIFFERENT PORTS
- PEAK AND AVERAGE POWER CAPABILITY
- OPTIMUM WEIGHT (CORRECTLY DESIGNED MAGNETIC BIASING CIRCUIT AND COOLING SYSTEM, IF REQUIRED)
- FREEDOM FROM NONLINEARITIES THAT WILL DETERIORATE PERFORMANCE

DUMMY LOADS
- FREQUENCY OF OPERATION
- MAXIMUM VSWR
- POWER CAPABILITY (AVERAGE AND PEAK)
- SIZE
- WEIGHT
- COOLING SYSTEM (IF REQUIRED)

SWITCHES
- FREQUENCY RANGE
- INSERTION LOSS
- VSWR
- ISOLATION TO THE NONOPERATION PORT
- POWER CAPABILITY (PEAK AND AVERAGE) RF
- SWITCHING SPEED
- HOLDING POWER, IF ANY
- REQUIRED VOLTAGE AND CURRENT
- SIZE AND WEIGHT

DIRECTIONAL COUPLERS

TYPE: DUAL, CROSSGUIDE, BROADWALL, SIDE WALL, LOOP, ETC
- FREQUENCY RANGE
- COUPLING VALUE
- VSWR (PRIMARY AND SECONDARY LINE)
- DIRECTIVITY
- COUPLING SENSITIVITY WITH FREQUENCY
- POWER CAPABILITY
- SIZE AND WEIGHT

MIL Handbook 216 also establishes electrical performance parameters for microwave components—frequency range, power capability, insertion loss, VSWR, switching speed, and attenuation. Waveguides and their support hardware, however, must conform to far more demanding mechanical requirements than those for conventional electronic components. **Table 2** lists the important electrical and mechanical parameters for a variety of EW radar-system microwave components.

The mechanical dimensions and tolerances of a waveguide control its fundamental propagation mode, attenuation, and insertion loss. Attenuation and insertion-loss characteristics per unit length are a function of the waveguide's wall finish. The guides' internal cross section defines the frequency spectrum that will propagate in the fundamental mode. Mode purity—the ability of a waveguide to transmit RF energy in the fundamental or primary mode—is a function of how well the manufacturer maintains the cross-section dimensions.

Because a waveguide must satisfy very precise mechanical requirements, its success or failure in an EW radar system hinges on its manufacture. After machining, the waveguide must go through a deburring process, which removes jagged edges and stray metal parts. Deburring is a critical procedure because waveguides must have clearly defined, sharp edges in order to meet their electrical specifications. On the waveguide openings, for example, any rounding that exceeds specified tolerances will degrade electrical performance. The dimensions of the coupling holes are also critical, because the holes determine the guide's coupling characteristics. Improper deburring can enlarge a hole to the point where it will critically alter the guide's coupling performance.

Further, waveguides and supporting components that require plating must be plated carefully. Improper

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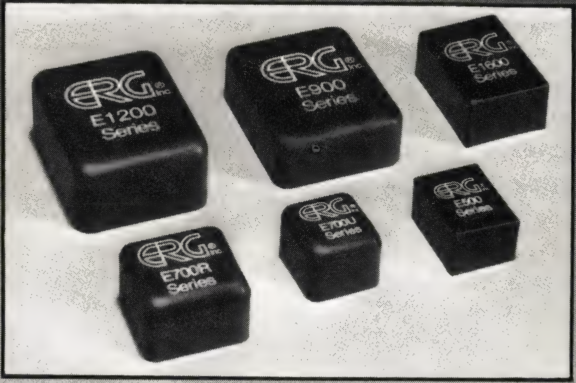

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CIRCLE NO 95

plating can easily change hole dimensions and wall thicknesses. If the plating increases the wall thickness slightly, or alters a coupling hole diameter in a directional coupler, the device could easily fail to meet its electrical specifications.

Besides consulting MIL Handbook 216, it's a good idea to refer to the Electronic Industries Association (EIA) standards for microwave transmission lines and components. EIA standards are consistent with those of MIL Handbook 216, but they also describe installation and deployment practices for waveguides. The EIA information will help you avoid improper waveguide installation, which could deform a waveguide, altering its characteristics and rendering it useless for the effective propagation of electrical energy. **EDN**

Author's biographies

John McCrea is executive vice president of Waveline Inc (West Caldwell, NJ). He is actively involved in acquiring new product lines to complement the company's off-the-shelf circulator/isolator products and waveguide passive components. In his leisure hours, John enjoys biking, swimming, and personal computers.

Charlie Schumann heads the electrical engineering department at Waveline Inc (West Caldwell, NJ). He is currently responsible for expanding the company's line of ridgeguide components, and he also oversees the development and design of new passive component products. In his spare time, Charlie dabbles in photography and enjoys playing bridge.

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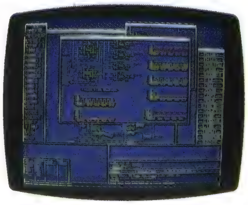

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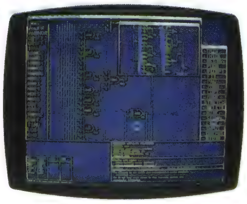

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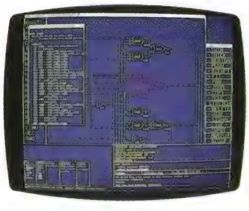

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CIRCLE NO 98

Use CMOS DACs to generate sine waves

You can use microprocessors in combination with D/A converters to generate sinusoidal waveforms with controllable and repeatable characteristics. One technique uses EPROM look-up tables to store sine-wave values; another method treats D/A converters as μP-controlled potentiometers in a classic, active RC-oscillator circuit.

John Wynne and Mike Byrne,
Analog Devices Semiconductor

Many analog-signal-processing, telemetry, and data-encoding applications require the generation of sinusoidal signals that have low harmonic content. Although you could use a number of purely linear techniques, circuits, and complete ICs to produce such low-distortion waveforms, these linear methods don't afford you digital control of the generated waveforms. By using D/A converters to create sinusoidal waveforms, however, you can obtain digital control of the waveforms. The following sections discuss three possible techniques for producing sine waves with D/A converters and present application examples that illustrate the techniques.

In two of the application examples, a D/A converter uses data from a look-up table that contains sine-wave amplitude and phase-angle information. The third example uses D/A converters as digitally controlled resistances in a classic, RC-oscillator configuration. In sine-wave generators using a look-up table, an up counter, driven at a given clock rate, scans the data in the look-up table and feeds the data to the D/A converter. The D/A converter then generates the sampled waveform, and a lowpass filter smoothes it.

Choose counter rates carefully

Before moving on to the concrete design examples, consider some general aspects of frequency control in look-up-table configurations. In a sine-wave generator using an up counter, a look-up table, and a D/A converter, it would appear that the easiest way to change the generator's output frequency is to increase the counter's clock rate. Changing this fundamental sampling frequency, however, has severe implications for the output filter. In digital audio, for example, a fixed sampling frequency is a must. Not only does the nonvarying frequency allow for synchronization of every component in the digital-audio chain, but it also means you can use filters of fixed response. If the sampling frequency were to vary, the alias frequencies would also vary. To eliminate alias frequencies, then, you'd need a programmable, high-order lowpass filter, which would be a complicated and expensive device.

To double the output frequency while maintaining a

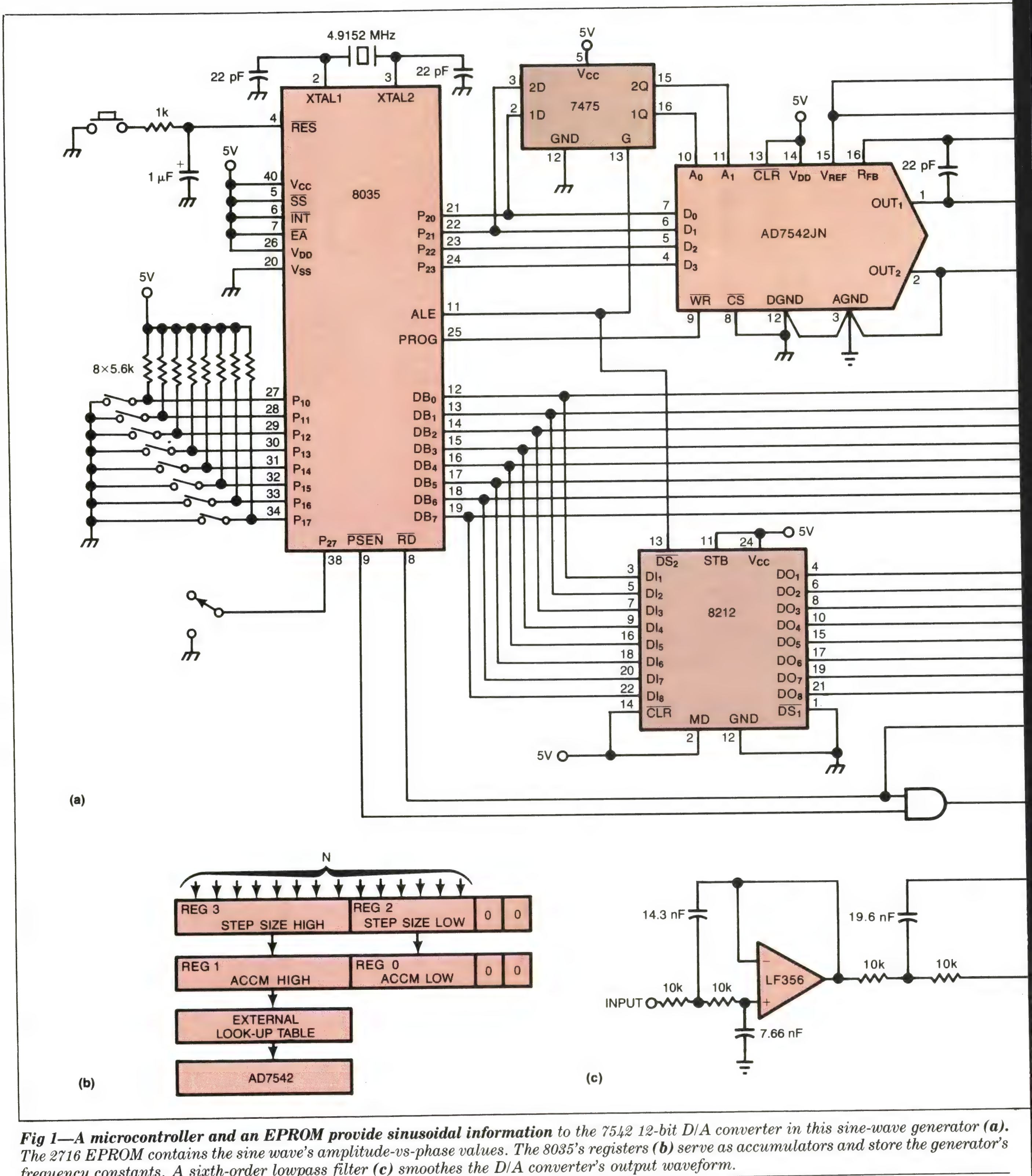
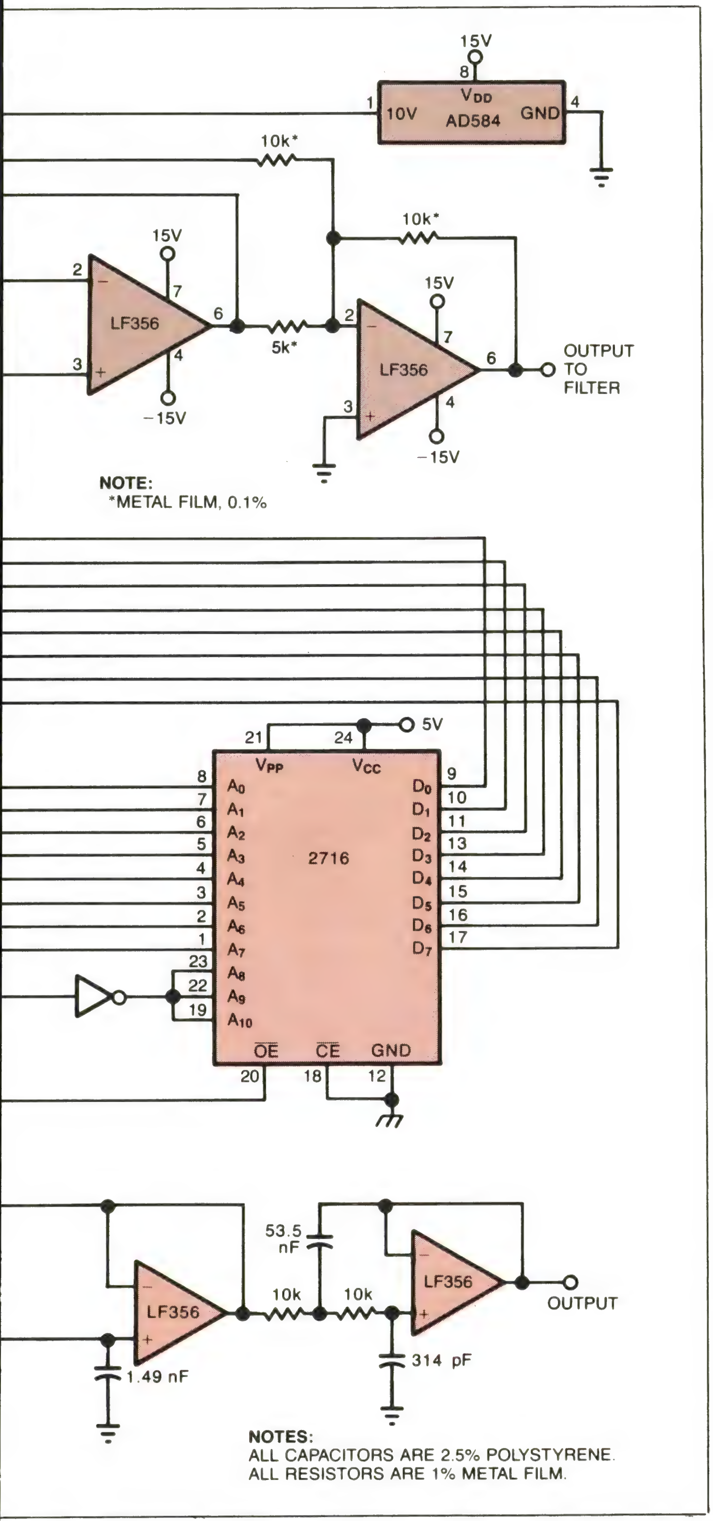


***Fig 1—A microcontroller and an EPROM provide sinusoidal information** to the 7542 12-bit D/A converter in this sine-wave generator **(a)**. The 2716 EPROM contains the sine wave's amplitude-vs-phase values. The 8035's registers **(b)** serve as accumulators and store the generator's frequency constants. A sixth-order lowpass filter **(c)** smoothes the D/A converter's output waveform.*

Using D/A converters to generate sine waves borrows techniques from both the digital and the analog worlds. As usual, μPs perform the management functions.



constant clock frequency, you can configure the software that loads the counter to increase the counter by two steps, instead of one, per loop. The counter thus fills and rolls over twice as quickly, thereby doubling the output frequency. Similarly, any integer that's a multiple of the initial counter stepping constant produces a corresponding multiplication of the output frequency.

The resolution required in the output signal determines the number of bits (m) required in the counter (or accumulator). The number of possible output-signal frequencies is 2^{m-1}, and the spacing between them is inversely proportional to 2^m. The generated output frequency is given by the equation $f_S = Nf_C/2^m$, where N is the constant that establishes the output frequency, f_C is the frequency of executing the loop (the sampling frequency), and m is the number of bits in the counter or accumulator. Assume, for example, that you're using a 14-bit accumulator and you need 1-Hz resolution in the output signal.

Choosing a base-frequency constant ($f_C/2^m$) of 1 to produce a 1-Hz output signal ensures that the frequency constant N always equals the output frequency. Thus, for a 14-bit counter to increase in single steps and roll over to zero once per second, you need a sampling rate of 2^{14} samples/sec (ie, a sampling frequency of 16,384 Hz). Each timing loop executes in 61.035 μsec.

μC controls sine waves

The circuit in **Fig 1a** shows how you can use a look-up table to generate sinusoidal signals. The 8-bit 8035 microcontroller (from the MCS-48 family) is the central controller in this programmable sine-wave generator. To provide the needed internal machine cycle time, the 8035 divides the external crystal's frequency by 15. A 4.9155-MHz crystal, therefore, yields a machine cycle time of 3.056 μsec, or 20 machine cycles per timing loop. You must tailor any branch in the program, however, to ensure that a complete loop through the program always takes 20 machine cycles.

The 8035's architecture limits the external look-up table's capacity to 256 entries. Thus, 256 bytes encode the sine function's 360° in 1.406° steps. Placing the full 360° in the look-up table simplifies the software at the expense of increased distortion in the output. **Fig 2** shows the Basic program (for an AIM-65 computer) that generates the sine-wave look-up table. The program takes into consideration the AD7542's bipolar operation and offset-binary coding. To keep the output waveform symmetrical around 0V, address FF_{HEX}

By using D/A converters to create sinusoidal waveforms, you can obtain digital control of the waveforms.

```
L=3840
FOR X=0 TO 255
LET A=SIN[(X*1.40625)/57.2958]
LET Y=INT(128.5+127*A)
POKE L,Y
LET L=L+1
NEXT X
END
```

Fig 2—This simple Basic program loads the sine-wave look-up table *into the 2716 EPROM in the circuit in* ***Fig 1a.*** *The program takes the D/A converter's bipolar operation and offset-binary coding into account.*

TABLE 1—DISTORTION VS OUTPUT FREQUENCY

INPUT FREQUENCY CONSTANT	OUTPUT FREQUENCY (Hz)	TOTAL HARMONIC DISTORTION (dB)
0	0	NA
1	1	−48
16	16	−48
17	17	−48
32	32	−52.6
33	33	−48
64	64	−54.8
65	65	−43
128	128.01	−56.2
129	129.01	−44.7
256	256.02	−54.6
257	257.02	−45.2
512	512.05	−55.4
513	513.05	−44.1
1024	1024.1	−55
1025	1025.1	−45
2048	2048.2	−52.4
2049	2049.2	−44.8
4096	4096.4	−57
4097	4097.4	−47

stores the greatest positive amplitude ($V_{REF}-1$ LSB) at 90° phase angle, and 01_{HEX} stores the greatest negative excursion ($-V_{REF}$) at 270°.

Fig 1b shows the arrangement of the registers within the 8035. Two 8-bit registers, REG 0 and REG 1, serve as the accumulator; REG 0 is the less significant. Registers REG 2 and REG 3 store the frequency constant N; REG 2 is the less significant. Both the 14-bit accumulator's contents and the 14-bit frequency constant occupy the most significant 14 bits of their respective 16-bit register pairs. The high byte of the 14-bit accumulator is the pointer for accessing the look-up table. As with the Basic program, the look-up table's arrangement takes into account the AD7542's bipolar operation and offset-binary coding. The AD7542 D/A converter is a double-buffered, 12-bit D/A converter that accepts input data in the form of 4-bit nibbles.

Address pins A_1 and A_0 of the AD7542 address the three 4-bit input registers and transfer the data to the D/A converter's output register. The rising edge of the control signal $\overline{WR}$ synchronizes all data-loading or data-transfer operations. The 2716 EPROM contains both the program and the sine look-up table for the 8035. The program memory is external and starts at location 000_{HEX}, the address to which the processor vectors after a reset. The look-up table serves as external data memory and occupies the highest page of the 2716, starting at address 700_{HEX}.

Bit 7 of port 2 differentiates between the high and low bytes of the right-justified frequency constant N, which loads in through port 1. A low level on P_{27} indicates that the low byte (8 LSBs) is present on P_{17} to P_{10}, and a high level on P_{27} indicates that the high byte (6 LSBs) is present on P_{15} to P_{10}. For the program to work correctly, the low byte of the frequency constant —with P_{27} low—must be present on port 1 before a reset appears. Almost immediately after a reset appears, the low byte of the frequency constant loads into port 1 and the program enters a loop that causes the high byte to load into port 1. The program exits the loop when P_{27} goes high (signifying the presence of the high byte). The μC next shifts the frequency constant two places to the left to position it properly in registers REG 2 and REG 3 before the program enters the frequency-synthesis loop.

All communications between the 8035 and the AD7542 take place over P_{20} to P_{23}. The interface uses only the transfer-accumulator-to-port instructions. Each transfer consists of two 4-bit nibbles; the first contains the op code and port address, and the second contains the four bits of data. A high-to-low transition of the PROG line indicates that address and op-code information are present on P_{20} to P_{23}. Simultaneously, the falling edge of ALE latches the port address into the 7475 latch. When the PROG line returns to the high state, the 4-bit-wide bus contains valid data. To load the data into the 7542, the PROG line drives the $\overline{WR}$ input.

The sixth-order lowpass active filter shown in **Fig 1c** smoothes the output waveform from the D/A converter. The filter provides 58-dB attenuation at 8 kHz. **Table 1** gives the relationship between total harmonic distortion and output frequency.

By using D/A converters, you can easily generate the sine waves needed to drive 3-phase motors. The circuit in **Fig 3** consists of a 2716 EPROM that contains sine-wave values in digital form, a counter that counts through the 2716's addresses, and logic that controls the counter and the loading of an AD7225 quad D/A converter. Three sections of the quad D/A converter provide the 3-phase sinusoidal outputs. Close matching and tracking of the three D/A converters in the AD7225 ensures close matching of the sine waves' amplitudes.

The AD7225 has double-buffered inputs; that is, it has four 8-bit input registers and four 8-bit D/A-converter registers. Only the data held in the D/A-converter registers determines the converters' outputs. In three clock cycles, the logic elements control the output of data from the 2716 and the successive loading of the AD7225's three input registers. The fourth clock cycle then loads the data from the input registers to the corresponding D/A-converter registers, thereby effecting a simultaneous update of the three sine-wave outputs.

Three sets of codes (for three sine waves 120° out of phase) constitute the data stored in the 2716. The fourth address contains a redundant code that corresponds to the clock cycle for loading the D/A-converter registers. Having this redundant memory location simplifies the control logic, because it allows a one-to-one

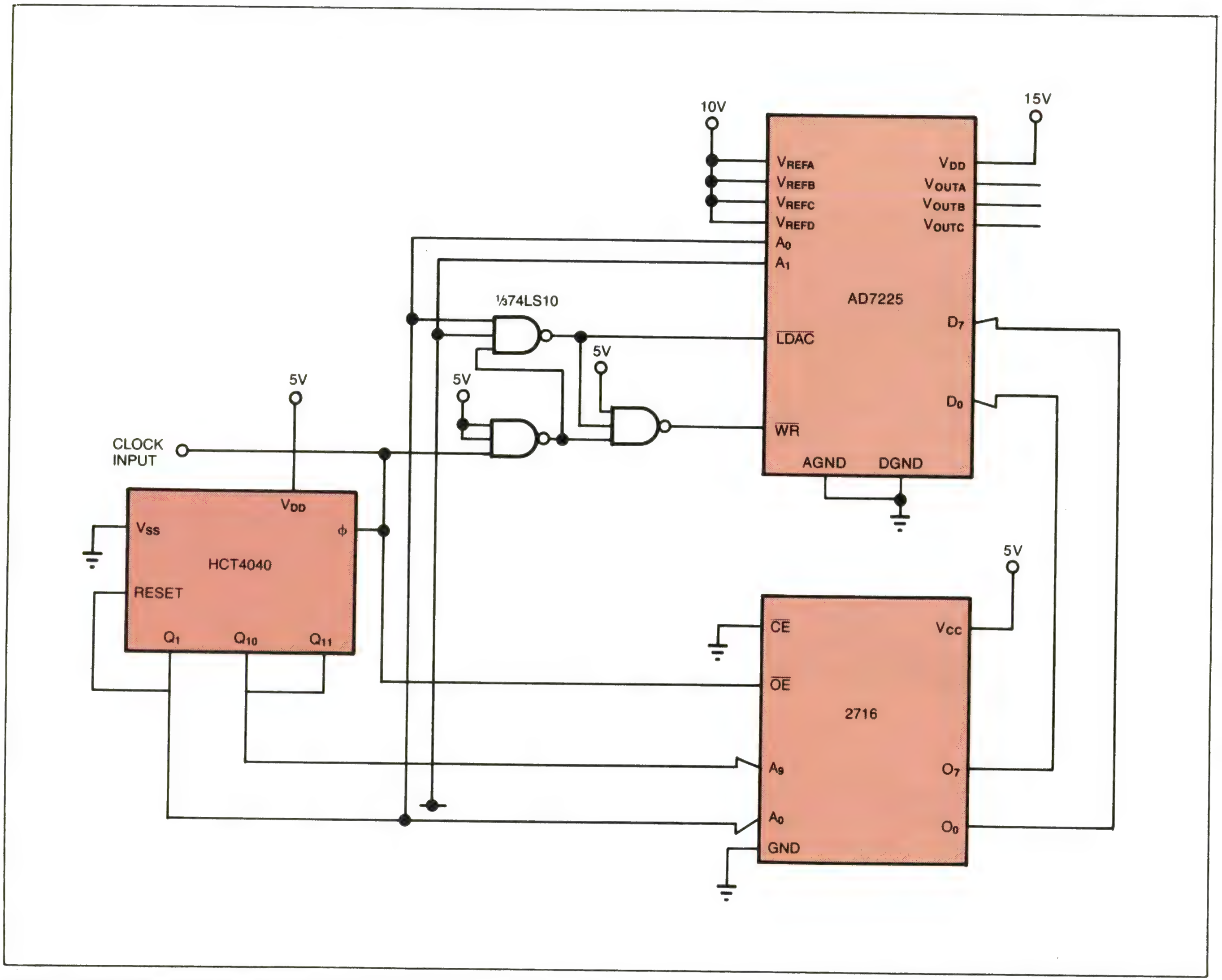


*Fig 3—**Three-phase sine waves are easy to generate** with this simple circuit. The HCT4040 counter steps through the addresses of the 2716 EPROM look-up table, and the look-up table's outputs drive three stages of the AD7225 quad D/A converter. The inherent tight matching of the three D/A converters' characteristics ensures close matching of the output sine-wave amplitudes.*

You can generate sine waves by using EPROM memory elements as μP-controlled look-up tables that supply sinusoidal phase-vs-amplitude information to the DAC.

relationship between EPROM addresses and AD7225 addresses. Assuming address x contains a code corresponding to 0°, then address x+1 contains a code corresponding to 120°, address x+2 has a code corresponding to 240°, and address x+3 contains the redundant code. The next set of addresses will update the sine value by the preprogrammed phase increment. Assuming you use a 256-element sine-wave table, x+4 equals 0°+1.4°.

To start the cycle, the 2716 loads the first address (x) into D/A converter A, address x+1 into D/A converter B, and address x+2 into D/A converter C. The counter implements a full address cycle for the three sine waves by stepping through the full look-up table in the EPROM. When the EPROM loads the data from the last address into the AD7225's D/A-converter registers, the counter resets and the cycle begins anew. **Fig 4** gives the Basic program (for an AIM-65 computer) for generating the code values for a 256-element sine-wave look-up table.

You must run the Basic program a total of three times to fill the locations in the sine-wave look-up table. The numerical values for the SIN function in code are in radians. To obtain fewer elements in the sine-wave table, you should add an appropriate STEP jump to line 2. For an 85-element table, for example, add "STEP 3" to line 2.

For a 256-element sine-wave table, the output frequency is the input clock frequency divided by 1024. In this application, spectral content is not very important and hence a constant sampling rate is not a major requirement. Varying the input clock frequency over the range of 5 kHz to 1.024 MHz causes the output frequency to vary over the range of 4 Hz to 1 kHz. **Fig 5** shows the typical waveforms that result, after you've filtered the outputs with single-pole RC filters. For a circuit using a 256-element sine-wave table, the total harmonic distortion is typically −48 dB for frequencies as high as 1.26 kHz.

```
INPUT "P"; P
FOR X = 0 TO 255
LET A = SIN[(X*1.40625 + P)/57.2958]
LET Y = INT(128.5 + 127*A)
POKE L,Y
LET L = L + 4
NEXT X
END
```

NOTES:
L = 3328 AND P = 0 FOR FIRST SINE WAVE.
L = 3329 AND P = 120 FOR SECOND SINE WAVE.
L = 3330 AND P = 240 FOR THIRD SINE WAVE.

***Fig 4—This Basic program manages all three sine waves** by using data from the 2716 look-up-table EPROM in **Fig 3**. The data stored in the look-up table consists of three sets of codes, one each for three sine waves 120° out of phase. You run the Basic program three times to fill the EPROM's locations. To obtain a look-up table that has fewer elements, add a STEP instruction to line 2.*

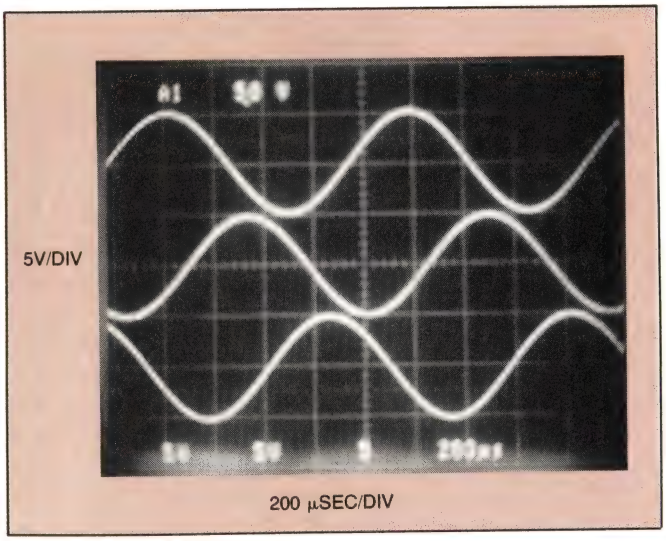


***Fig 5—The 3-phase outputs of the circuit in Fig 3** are shown in this scope photo. The waveforms were obtained by using single-pole filters to filter the D/A converters' outputs.*

The limiting factor for the frequency range is the 2716 EPROM's 450-nsec data-access time. To increase the range, you should replace the 2716 with an EPROM having a faster access time. Alternatively, if a constant sampling rate is important, using a look-up table with fewer elements increases the frequency of the output sine waves, because the time it takes to cycle through a full look-up table decreases. Note that you must take care that the filters used on the three D/A-converter outputs do not introduce different phase shifts in the outputs.

Digital and analog work together

Sine waves generated by circuits using look-up tables, such as the application circuits already discussed, are composed of discrete stairsteps; the number of steps in a circuit depends on the resolution of the circuit's D/A converter. You can also produce sine waves by using D/A converters in purely linear circuits, however. The state-variable oscillator in **Fig 6**, for example, uses two 12-bit D/A converters as digitally

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The ladder network of a CMOS DAC acts as a digitally controlled variable resistor in an active RC oscillator; the DAC's digital inputs set the frequency.

programmable resistors in the IC_2 and IC_3 integrator stages. The circuit's oscillation frequency is given by the equation

$$f = \frac{1}{2\pi}\sqrt{\frac{R_6}{R_5}}\sqrt{\frac{1}{R_{EQ1}C_1R_{EQ2}C_2}},$$

where R_{EQ1} and R_{EQ2} are the equivalent resistances of the two D/A converters. The same digital code drives the two converters. If $C_1=C_2$ and $R_5=R_6$, the expression reduces to

$$f = \frac{1}{2\pi C}\sqrt{\frac{1}{R_{EQ1}R_{EQ2}}}.$$

Assuming that n is the base-10 number of possible D/A-converter codes (4096 for the 12-bit converters shown) and N is the base-10 value of the applied binary code, $R_{EQ1}=(2^n/N)R_{LAD1}$ and $R_{EQ2}=(2^n/N)R_{LAD2}$, where R_{LAD1} and R_{LAD2} are the ladder resistances of the two converters. The frequency expression then becomes

$$f = \frac{1}{2\pi C}\sqrt{\frac{(N/2^n)^2}{R_{LAD1}R_{LAD2}}}.$$

If we define a constant $D=N/2^n$, the frequency is

$$f = \frac{D}{2\pi C}\frac{1}{\sqrt{R_{LAD1}R_{LAD2}}}$$
$$= \frac{1}{2\pi}\frac{D}{CR_{LAD}\sqrt{M}},$$

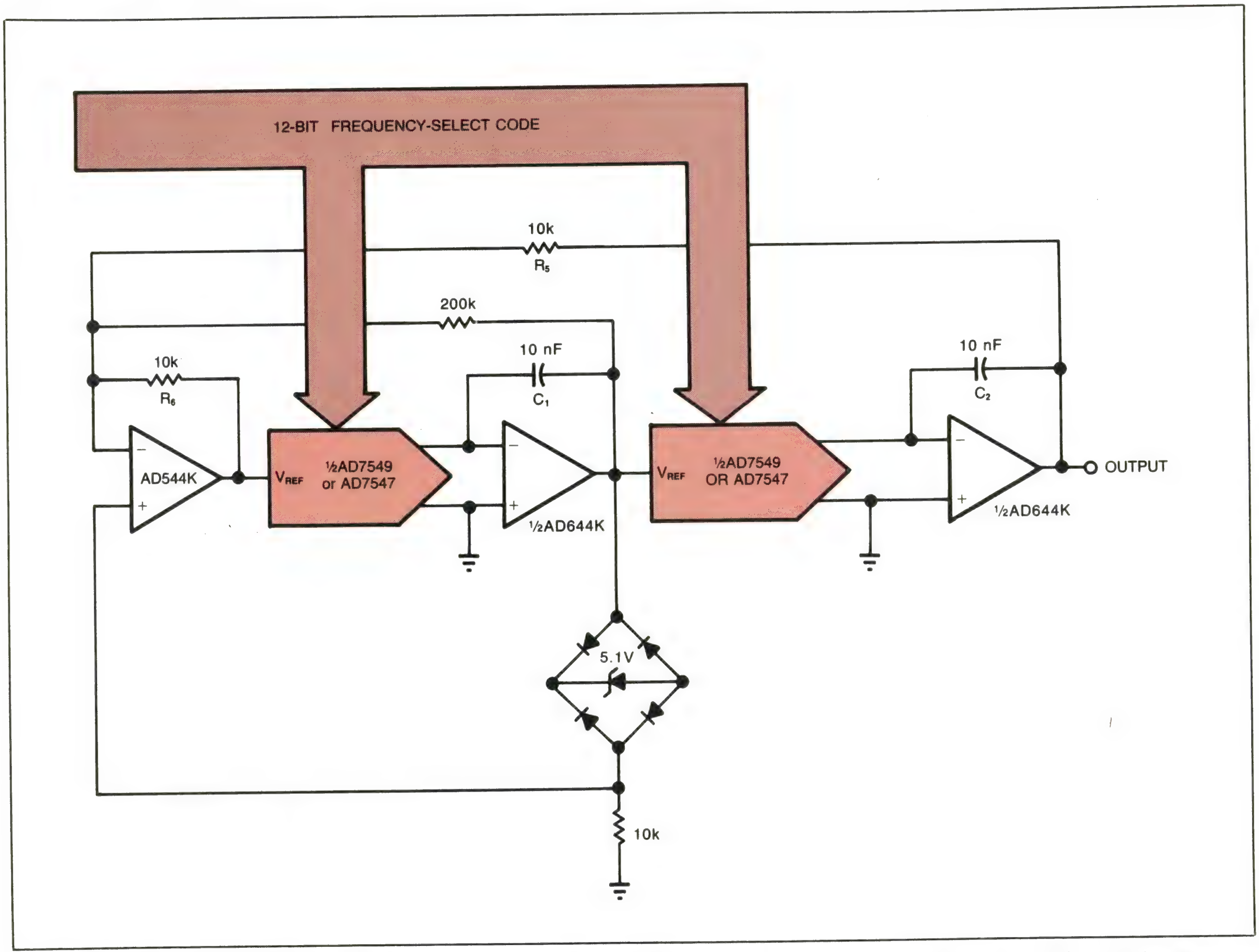
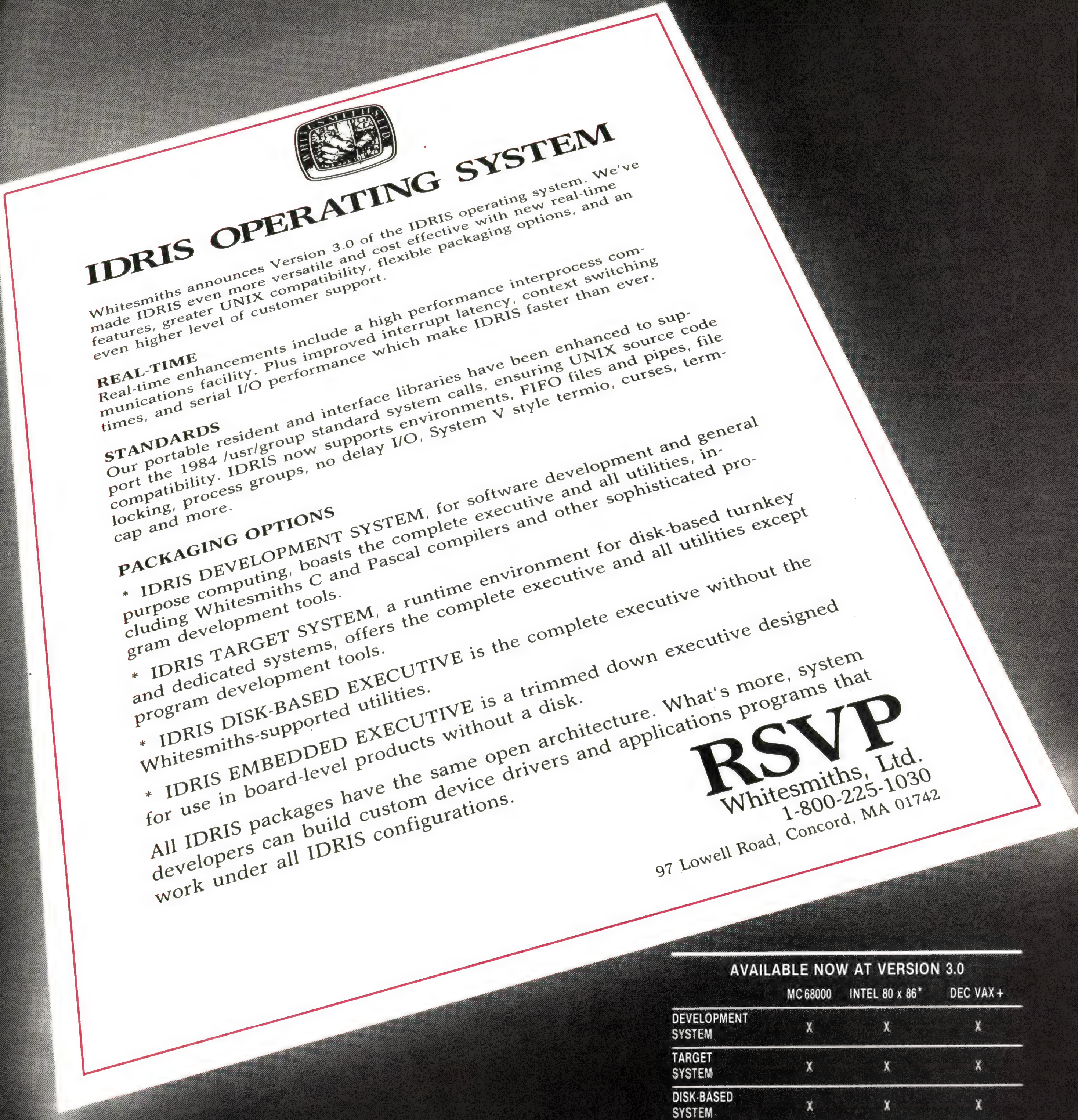


***Fig 6—Use a microprocessor to control D/A converters' ladder resistance** in this state-variable oscillator. The D/A converters serve as variable resistors that set the circuit's oscillation frequency.*



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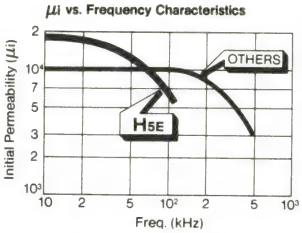

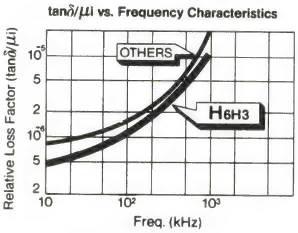

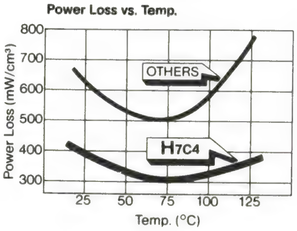

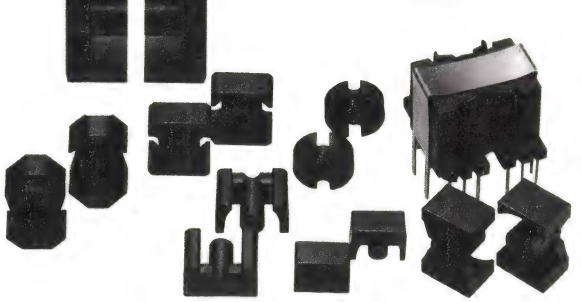

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where M is the mismatch ratio (R_{LAD2}/R_{LAD1}) of the ladder resistances in the two D/A converters.

For an oscillator with the values shown in **Fig 6,** the output frequency varies from 0 Hz (N=0) to 1.46 kHz ($N=4095_{10}$) in steps of approximately 0.358 Hz per bit. The amplitude of the oscillator's output signal is 10V p-p, and this amplitude is constant over the entire frequency span. Total harmonic distortion of the output signal, also constant over the whole frequency range, is −55 dB. **EDN**

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Authors' biographies

John Wynne, a senior applications engineer at Analog Devices Semiconductor (Wilmington, MA), is the supervisor of the CMOS applications department. A 6-year employee of ADI, he previously worked at VEC (Dublin, Ireland) and Sperry Gyroscope (Bracknell, England). Wynne holds a degree in electronic engineering from the Devin Street College of Technology in Dublin. A graduate member of the Institute of Electronic and Radio Engineers, Wynne enjoys music, reading, and squash in his spare time.

Mike Byrne, an applications engineer at Analog Devices Semiconductor (Wilmington, MA), has worked at the company for five years. Byrne holds a BSc degree in electronic systems from the National Institute for Higher Education in Limerick, Ireland. His hobbies include outdoor sports and music.

Article Interest Quotient (Circle One)
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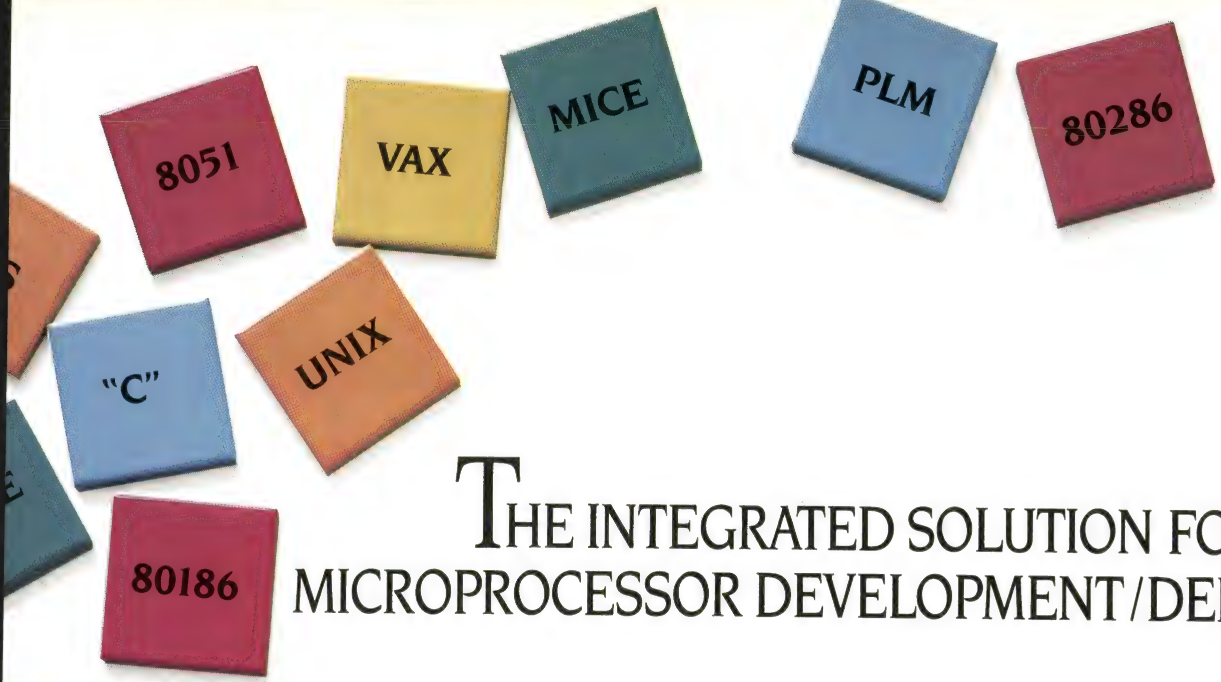

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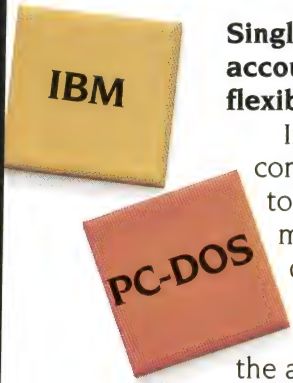

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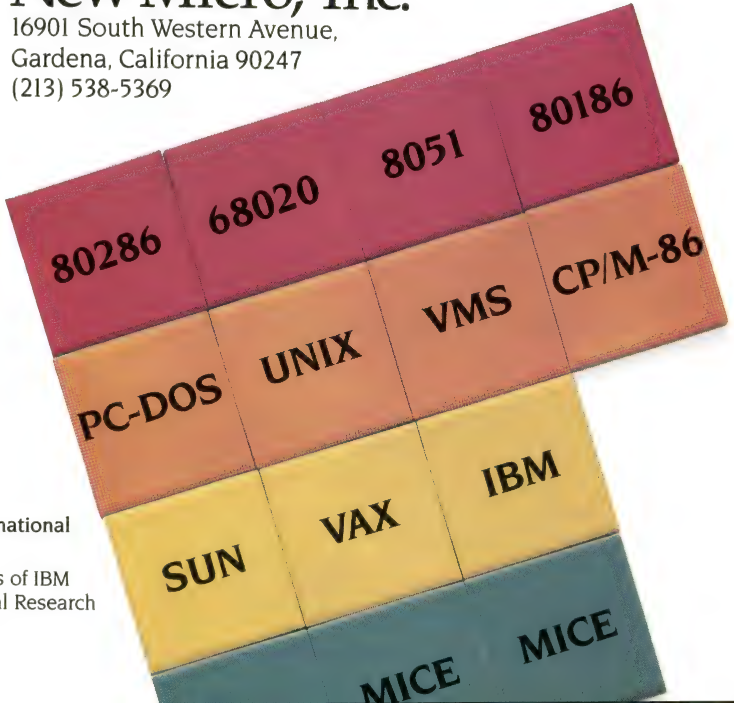

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CIRCLE NO 102

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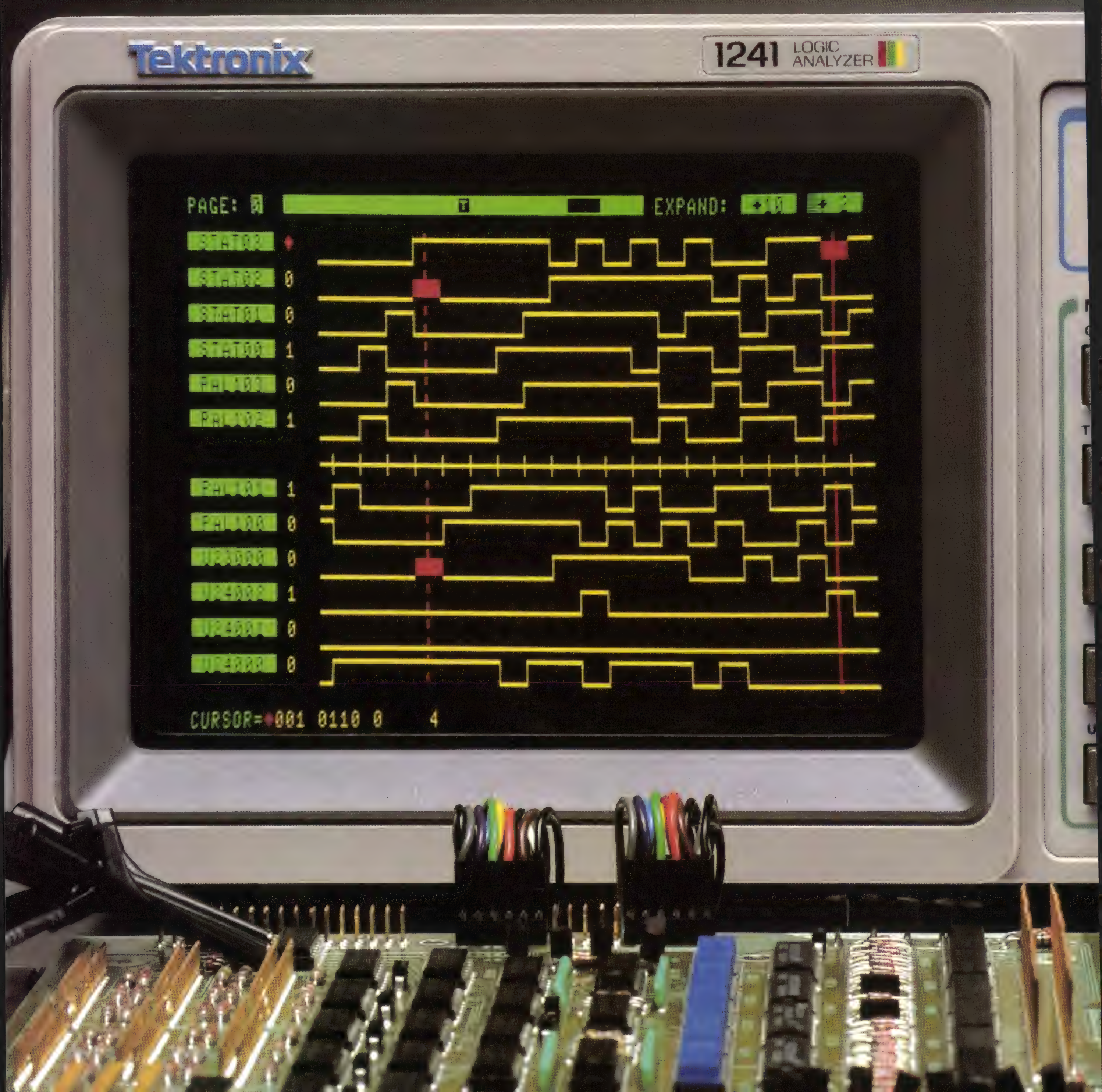

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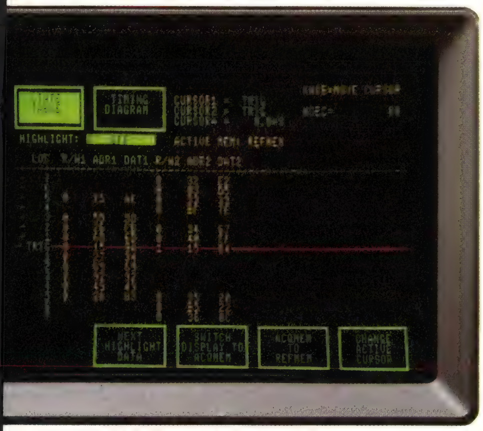

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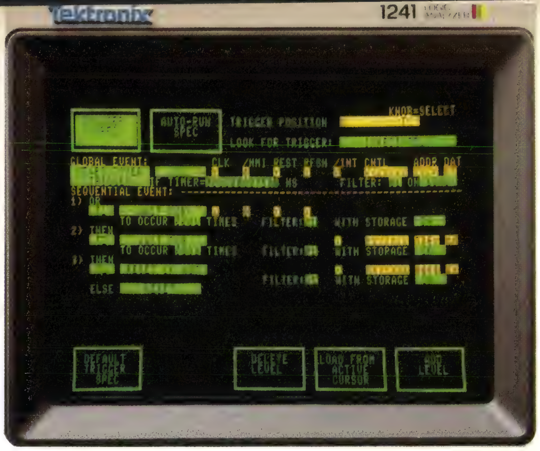

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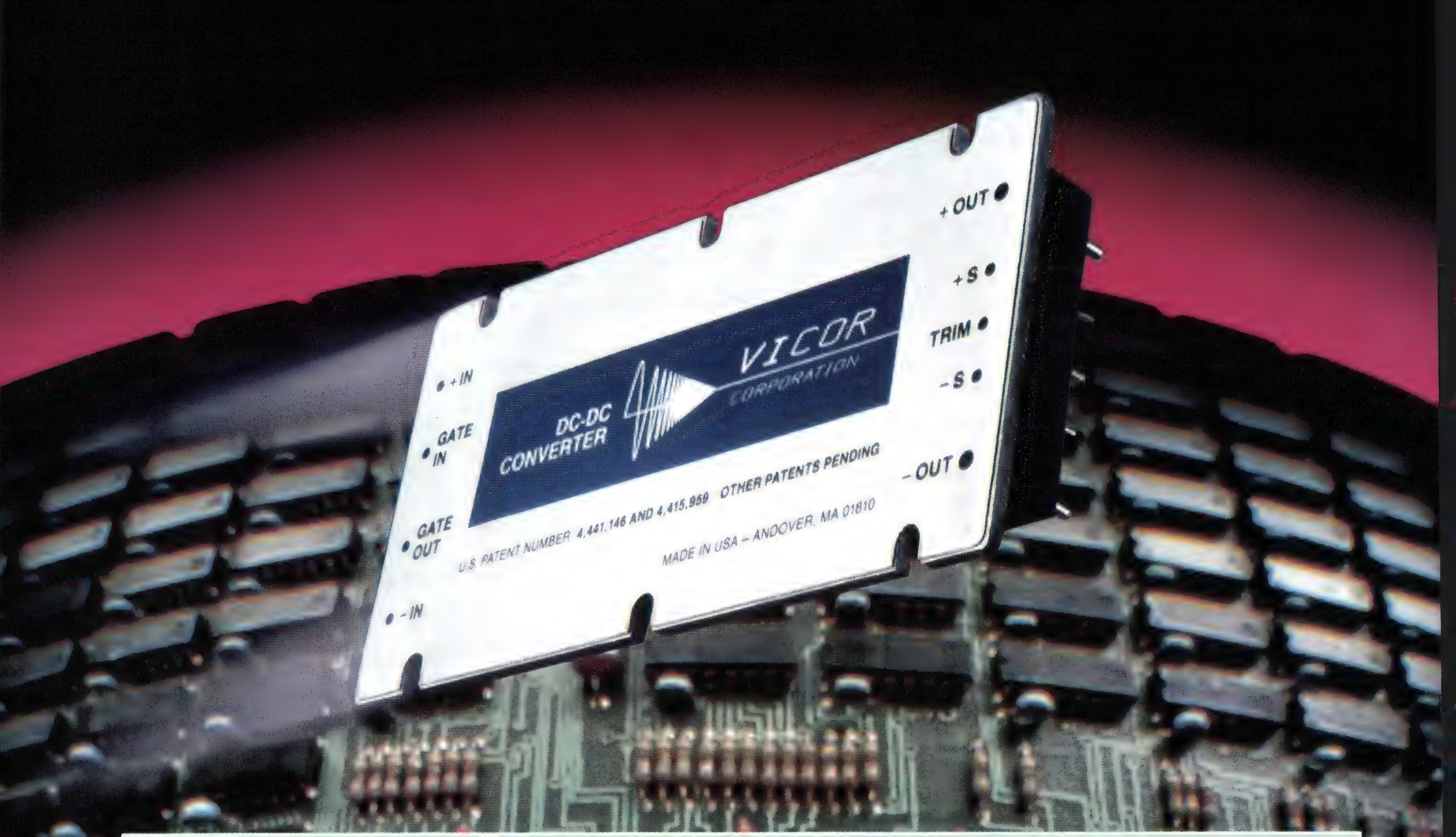
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The MTP10N10M SENSEFET is a milestone in power MOSFET technology. So simple, so straightforward in concept, yet so outstanding, we patented it.* And we're incorporating it into many of our leading-edge power semiconductors.

A mirror image of efficiency.

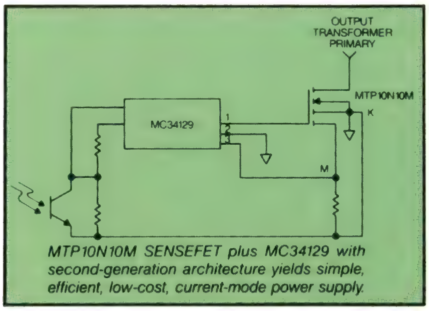
SENSEFETs are the first, multi-function powerFETs to provide direct access to a few, isolated source cells to measure current. Inherently-matched to the thousands of others they represent, acting separately through their own pins, these cells conduct, or mirror, only a miniscule fraction of drain current out of the mirror (M) terminal to generate voltage for comparator referencing.

This allows use of nominal value, low-cost, low-power resistors instead of large, inefficient and expensive power types.

Typical MTP10N10M sense ratio is greater than 1,000 so the amount of sense current is more than three orders of magnitude less than the load current. That results in a thousand times less power dissipation when compared to conventional current sensing techniques. That's as efficient and lossless as you can get.

An easier way to control design.

A SENSEFET-switching power supply calling for 200 mV drop across the sense resistor to sense 10 A maximum current flow requires a small resistor of 36 ohms with a power dissipation of only 1.1 mW. Plus, no significant heat is generated near the powerFET. A conventional circuit requires a costly, 0.02 ohm unit, taking up to ½″ x 1″ of real estate and dissipating 2 W.



MTP10N10M SENSEFET plus MC34129 with second-generation architecture yields simple, efficient, low-cost, current-mode power supply.

Comparison of Current Sensing Techniques

	V_{sense}	I_{sense}	R_{sense}	Type Resistor	Pd
Conventional	0.2V	10A	0.02Ω	Wire Wound	2W
SENSEFET™	0.2V	5.6mA	36Ω	Film	1.1mW

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MIL-C-38999 Specification Test	Series III Requirements	Series IV Requirements
SINE VIBRATION Magnitude Duration Temperature Cycle	60 G 36 hours -55°C to 200°C	30 G 12 hours Ambient
RANDOM VIBRATION Magnitude Temperature	44.1 GRMS 200°C	44.1 GRMS Ambient
HUMIDITY after TEMPERATURE LIFE	10 days with temperature cycling	Not required
EXTERNAL BENDING MOMENT (Shell size 25)	1,000 in./lbs.	650 in./lbs

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CIRCLE NO 104

DESIGN IDEAS

EDITED BY TARLTON FLEMING

Circuit provides controllable resistance

H H Eck
Pulse Electronics Inc, Rockville, MD

The bipolar transistor Q_1 in **Fig 1** presents a linear, dependent resistance between nodes A and B. By extending the connections from IC_1, IC_2, and Q_1's base, you can remotely control a resistance value.

Nodes A and B may assume any voltage value within the output range of op amps IC_1 through IC_5, provided the voltage of node A is more positive than B. You set R_{AB} (the resistance between A and B) to its maximum value by adjusting R_B to its maximum. R_{AB} can't go to zero, but the divider action of R_K provides a lower (and adjustable) limit for the minimum value for R_{AB}. If R_B alone gives enough range, you may eliminate R_K and IC_4.

R_{AB} remains linear over a range exceeding 20:1. In the test configuration in **Fig 2**, $R_{AB}=0.061R_B\pm2\%$ as R_B varies from 34 to 825 kΩ.

For simplicity's sake, you can assign any convenient value to resistors R and R_K (eg, 5 kΩ) **(Fig 1).** To derive an expression for R_{AB}, note that $V_1=(V_A-V_B)$, $V_3=(V_A-0.6V-V_2)$, and $V_2=V_1/K$, where K is the ratio of R_K's wiper voltage to V_1. Then,

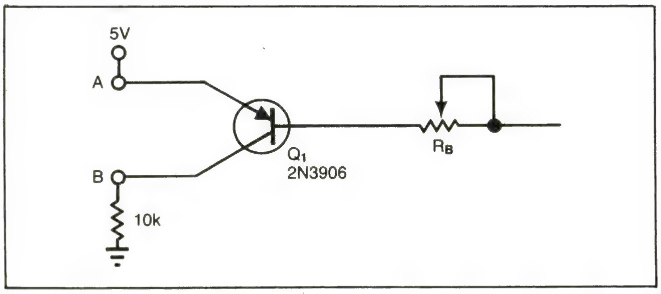


*Fig 2—**In this test configuration,** $R_{AB}=0.061R_B\pm2\%$ as R_B varies from 34 to 825 kΩ.*

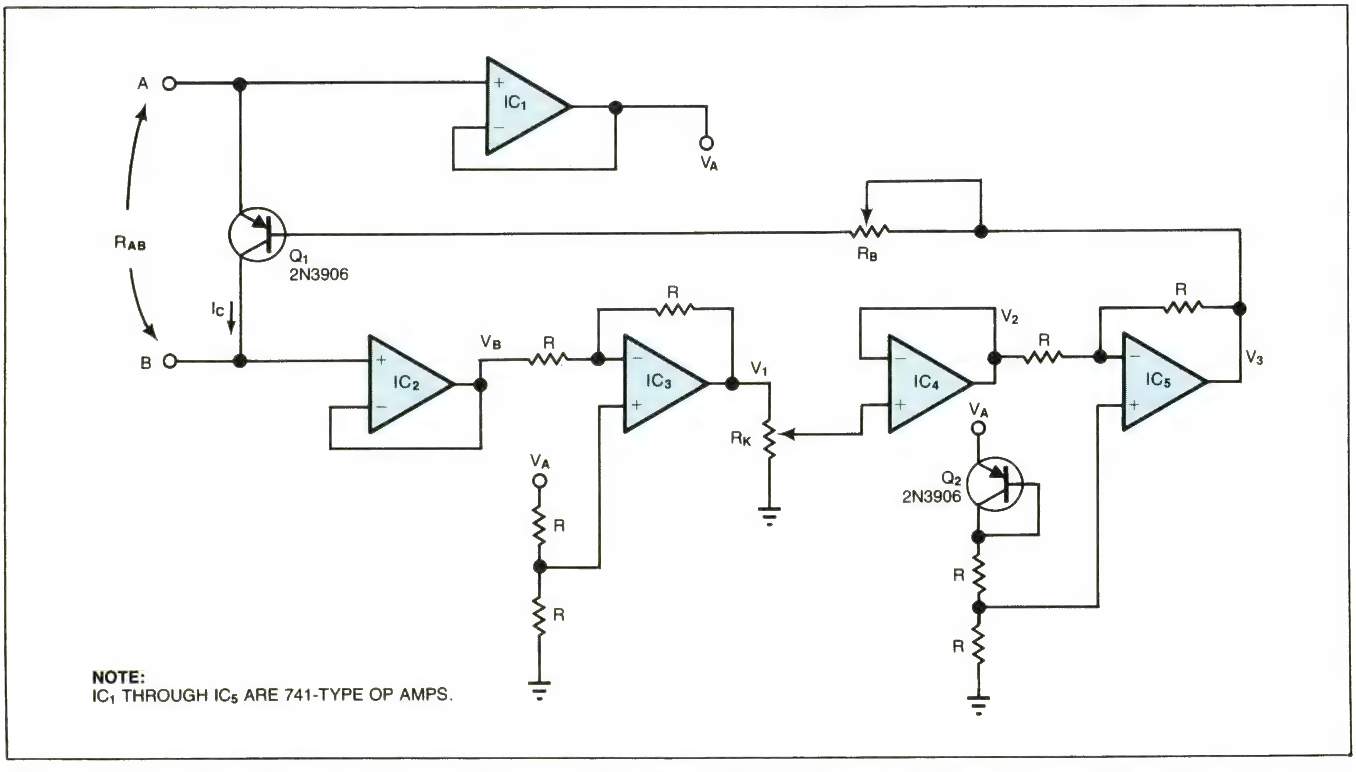
$$I_C=\beta I_B=\beta\left(\frac{V_A-0.6V-V_3}{R_B}\right)=\beta\left(\frac{V_A-V_B}{KR_B}\right),$$

where β is the transistor's short-circuit current gain. Assuming the transistor's emitter and collector currents are equal,

$$R_{AB}=\frac{V_A-V_B}{I_C}=\frac{KR_B}{\beta}.$$

EDN

To Vote For This Design, Circle No 748



NOTE:
IC_1 THROUGH IC_5 ARE 741-TYPE OP AMPS.

*Fig 1—**Resistance (R_{AB}) between nodes A and B** is a linear function of the wiper positions for potentiometers R_B and R_K.*

PLD provides chip select and wait states

Vineet Dujari
Advanced Micro Devices, Sunnyvale, CA

You can combine a memory-address decoder and wait-state generator in one 24-pin DIP by programming an AmPAL22V10 or equivalent device according to **Listing 1.** With this device, your microprocessor clock can accommodate the fastest memory chip in your system instead of the slowest.

The example in **Fig 1** is based on a Z80 CPU and assumes a memory system that includes two blocks of 16k-byte addresses (enabled by CS01 and CS23) and four blocks of 8k-byte addresses (enabled by CS4, CS5, CS6, and CS7). You can support other memory configurations by changing the outputs specified in the chip-select-decoder specification in **Listing 1.**

The AmPAL22V10 generates chip-select signals for the memory when the $\overline{\text{MREQ}}$ signal is active; in addition, it loads an appropriate count value in the wait-state counter at that time. This counter's high-level bit connects to the CPU's $\overline{\text{WAIT}}$ signal, so the CPU waits until the high-level bit is set before terminating that memory cycle. The internal CTSTATE signal determines if the counter is in the load or the count mode. This example inserts from zero to three wait states in every memory cycle. **EDN**

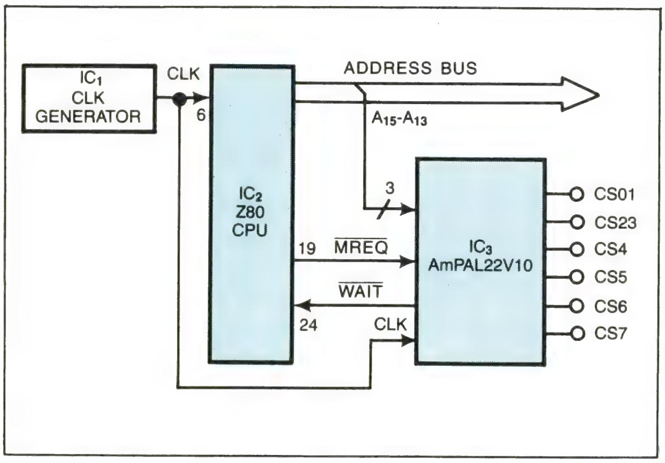


***Fig 1—An AmPAL22V10 chip** generates chip-select signals and wait states for the memory of a Z80-based system.*

To Vote For This Design, Circle No 749

LISTING 1

```
" A CHIP SELECT AND WAIT STATE GENERATOR "
" USING Am22V10 PAL FOR A Z80 SYSTEM. "

DEVICE CS_PLUS_WAIT_FOR_Z80 (PAL22V10)

PIN     CLK = 1                 " SYSTEM CLOCK INPUT "
        CS01 = 23               " CHIP SELECT FOR A15:A13 = 0 OR 1 "
        CS23 = 22               " CHIP SELECT FOR A15:A13 = 2 OR 3 "
        CS4 = 21                " CHIP SELECT FOR A15:A13 = 4 "
        CS5 = 14                " CHIP SELECT FOR A15:A13 = 5 "
        CS6 = 15                " CHIP SELECT FOR A15:A13 = 6 "
        CS7 = 16                " CHIP SELECT FOR A15:A13 = 7 "
        MREQ = 2                " MEMORY REQUEST SIGNAL "
        ADDR[15:13] = 5:3       " UPPER ADDRESS SIGNALS "
        CTSTATE = 17            " 0 : COUNT; 1 : LOAD "
        BIT[2:0] = 20:18;       " WAIT STATE COUNTER "

DEFINE WAIT = BIT[2];           " MSB OF COUNTER TO CPU WAIT- INPUT "

" CHIP SELECT DECODER SPECIFICATION FOLLOWS "

BEGIN
  IF ( /MREQ ) THEN
    BEGIN
      CASE ( ADDR[15:13] )
        BEGIN
          0) BEGIN
                CS01 = 0;       CS23 = 1;       CS4 = 1;
                CS5 = 1;        CS6 = 1;        CS7 = 1;
             END;
          1) BEGIN
                CS01 = 0;       CS23 = 1;       CS4 = 1;
                CS5 = 1;        CS6 = 1;        CS7 = 1;
             END;
          2) BEGIN
               CS01 = 1;        CS23 = 0;        CS4 = 1;
               CS5 = 1;         CS6 = 1;         CS7 = 1;
             END;
          3) BEGIN
               CS01 = 1;        CS23 = 0;        CS4 = 1;
               CS5 = 1;         CS6 = 1;         CS7 = 1;
             END;
          4) BEGIN
               CS01 = 1;        CS23 = 1;        CS4 = 0;
               CS5 = 1;         CS6 = 1;         CS7 = 1;
             END;
          5) BEGIN
               CS01 = 1;        CS23 = 1;        CS4 = 1;
               CS5 = 0;         CS6 = 1;         CS7 = 1;
             END;
          6) BEGIN
               CS01 = 1;        CS23 = 1;        CS4 = 1;
               CS5 = 1;         CS6 = 0;         CS7 = 1;
             END;
          7) BEGIN
               CS01 = 1;        CS23 = 1;        CS4 = 1;
               CS5 = 1;         CS6 = 1;         CS7 = 0;
             END;
        END;
    END;
  ELSE                            " WHEN MREQ- IS INACTIVE KEEP "
    BEGIN                         " ALL CHIP SELECT LINES INACTIVE "
      CS01 = 1;         CS23 = 1;        CS4 = 1;
      CS5 = 1;          CS6 = 1;         CS7 = 1;
    END;

 " FLIP FLOP TO REMEMBER COUNTER ACTIVE STATE "

   IF ( /MREQ ) THEN
     BEGIN
       CTSTATE := 0;
     END;
   ELSE
     BEGIN
       CTSTATE := 1;
     END;


 " WAIT STATE COUNTER SPECIFICATION FOLLOWS "

   IF ( /MREQ ) THEN
     BEGIN
       IF ( CTSTATE ) THEN         " LOAD COUNTER WITH A VALUE "
         BEGIN                     " DEPENDING ON THE UPPER "
           CASE ( ADDR[15:13] )    " ADDRESS BITS "
             BEGIN
               0) BIT[2:0] := 4;   " 4 : NO WAIT STATE "
               1) BIT[2:0] := 4;   " 3 : ONE WAIT STATE "
               2) BIT[2:0] := 3;   " 2 : TWO WAIT STATES "
               3) BIT[2:0] := 3;   " 1 : THREE WAIT STATES "
               4) BIT[2:0] := 2;
               5) BIT[2:0] := 2;
               6) BIT[2:0] := 1;
               7) BIT[2:0] := 1;
             END;
         END;
       ELSE                        " COUNT UP "
         BEGIN
           CASE ( BIT[2:0] )
             BEGIN
               0) BIT[2:0] := 1;
               1) BIT[2:0] := 2;
               2) BIT[2:0] := 3;
               3) BIT[2:0] := 4;
               4) BIT[2:0] := 5;
               5) BIT[2:0] := 6;
               6) BIT[2:0] := 7;
               7) BIT[2:0] := 0;
             END;
         END;
     END;
   ELSE
     BEGIN
       BIT[2:0] := 7;                       " KEEP WAIT INACTIVE "
     END;                                   " WHEN MREQ IS INACTIVE "
END.
```

High-gain amp yields low dc output offset

Christopher Paul and Leslie Burgner
Coherent Communications Systems Corp,
Hauppauge, NY

The digitally controlled audio amplifier in **Fig 1** exhibits high gain and a low variation in output offset voltage. Using the components shown, the circuit can provide a 50-dB gain with an error as low as ±0.2 dB for the 30- to 3000-Hz frequency range. For lower gains, you can obtain a similar level of error at higher frequencies. The variation of output offset voltage with gain changes is less than 15 mV.

Other digital-control schemes either can't achieve enough gain at high frequencies or exhibit an excessive variation of offset voltage with changing gain. For example, a circuit comprising a D/A converter and an op amp **(Fig 2)** features low output offset voltage, but a maximum gain of only 6 dB.

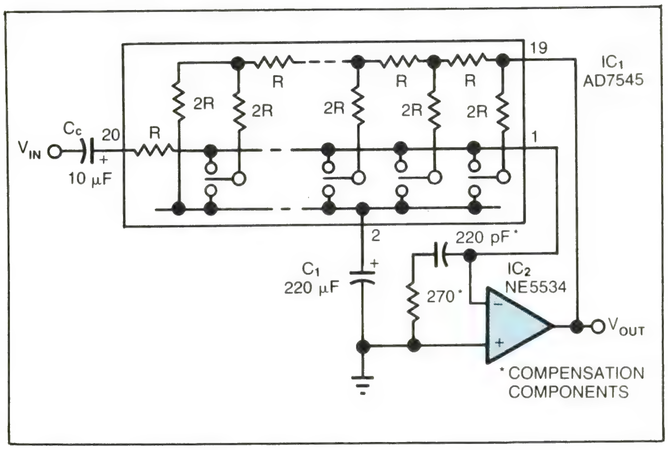


***Fig 1—By capacitively coupling both V_{IN}** and the D/A converter's ladder termination (AGND, pin 2), this digitally controlled audio amp can achieve an ac gain as high as 50 dB while limiting dc gain to 1. Consequently, the circuit's output offset variations with changing gain are 15 mV max; these variations are mostly a result of the amplifier's input-offset current flowing in the D/A converter's ladder network.*

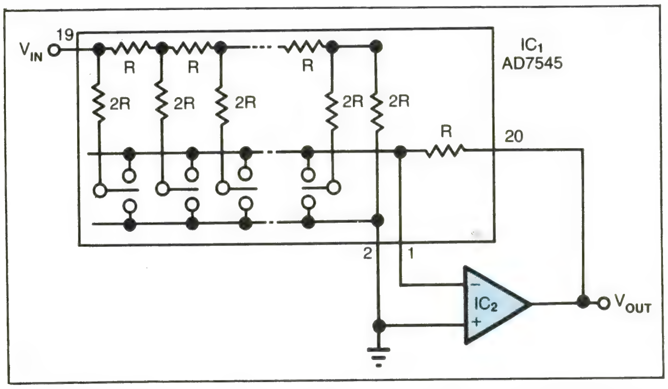


***Fig 2—This digitally controlled audio amp** exhibits low output-offset-voltage variations, but yields a gain of only 6 dB.*

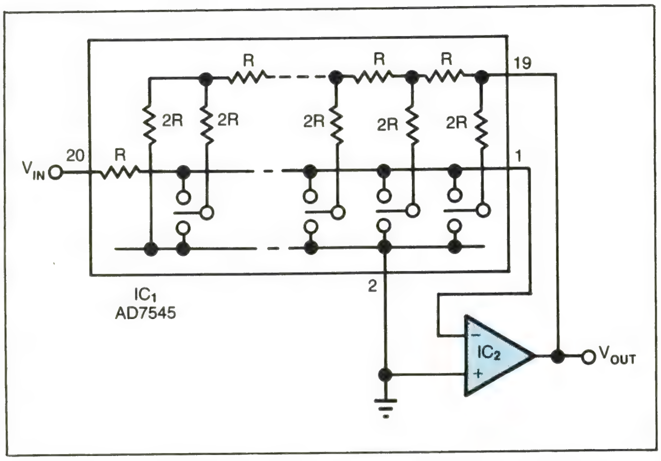


***Fig 3—Although it features high gain,** this digitally controlled audio amp's output offset voltage can vary several volts with gain changes.*

Fig 3, on the other hand, shows a D/A-converter ladder network in the feedback path of an op amp. This circuit yields high gain, but gain changes can cause several volts of variation in the output offset voltage (the op amp's input offset voltage is multiplied by the circuit's closed-loop gain). This circuit requires an op amp with low input offset voltage. The op amp also requires high open-loop gain to keep closed-loop gain errors low. It's difficult for a single op amp to satisfy these requirements.

The circuit in **Fig 1** overcomes the dc-offset problem of **Fig 3** by using ac coupling (through capacitor C_1) to connect the D/A converter's ladder network to ground. As a result, the op amp's input offset voltage is no longer multiplied by the circuit's closed-loop gain, which lessens the need for low offset voltage in the op amp. The op amp still requires high open-loop gain, however. The Signetics NE5534 is a good choice: It provides 80 dB of open-loop gain at 10 kHz.

For the values shown, **Fig 1**'s circuit operates at frequencies as low as 30 Hz; if you substitute higher-valued capacitors, it will operate at lower frequencies. Further, C_1 may have a low voltage rating because it operates at virtually 0V. **EDN**

(Ed Note: We are republishing this Design Idea because several errors appeared in the original edited version.)

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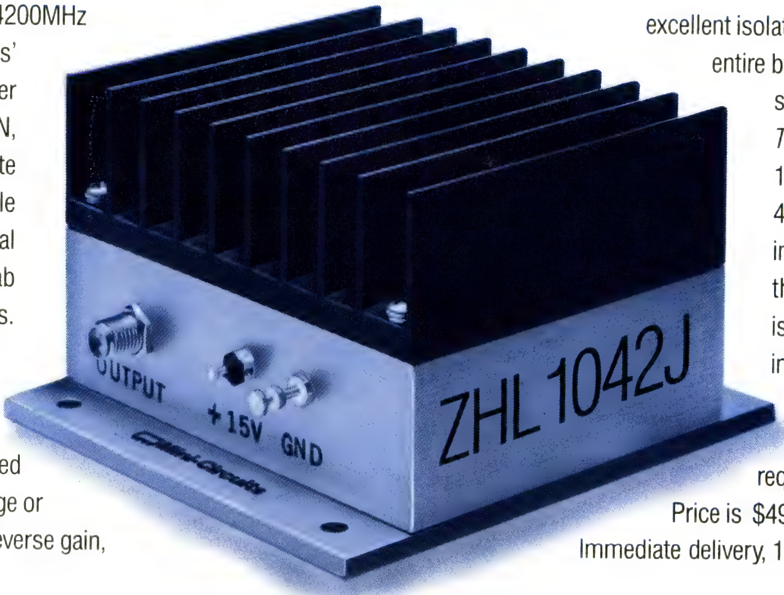

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CIRCLE NO 105

C106 REV. ORIG.

Z80 µP system utilizes an 8259 PIC

Cristian Constantinescu
Polytechnic Institute of Bucharest,
Bucharest, Romania

For Z80- or Z80A-based microprocessor systems that handle many vectored-priority interrupt lines, an 8259 (or 8259A or 8259-5) programmable interrupt controller (PIC) may offer better performance than the Z80 family's daisy-chain interrupt structure.

The Z80 µP operates in interrupt mode 0 (**Fig 1**). The external gates and the IC_2 flip-flop together generate three consecutive $\overline{INTA}$ pulses as required by the PIC to release a 3-byte Call instruction to the data bus. This instruction includes the Call op code and two address bytes for the interrupt's service routine.

To initiate an interrupt request, the µP's $\overline{M1}$ and

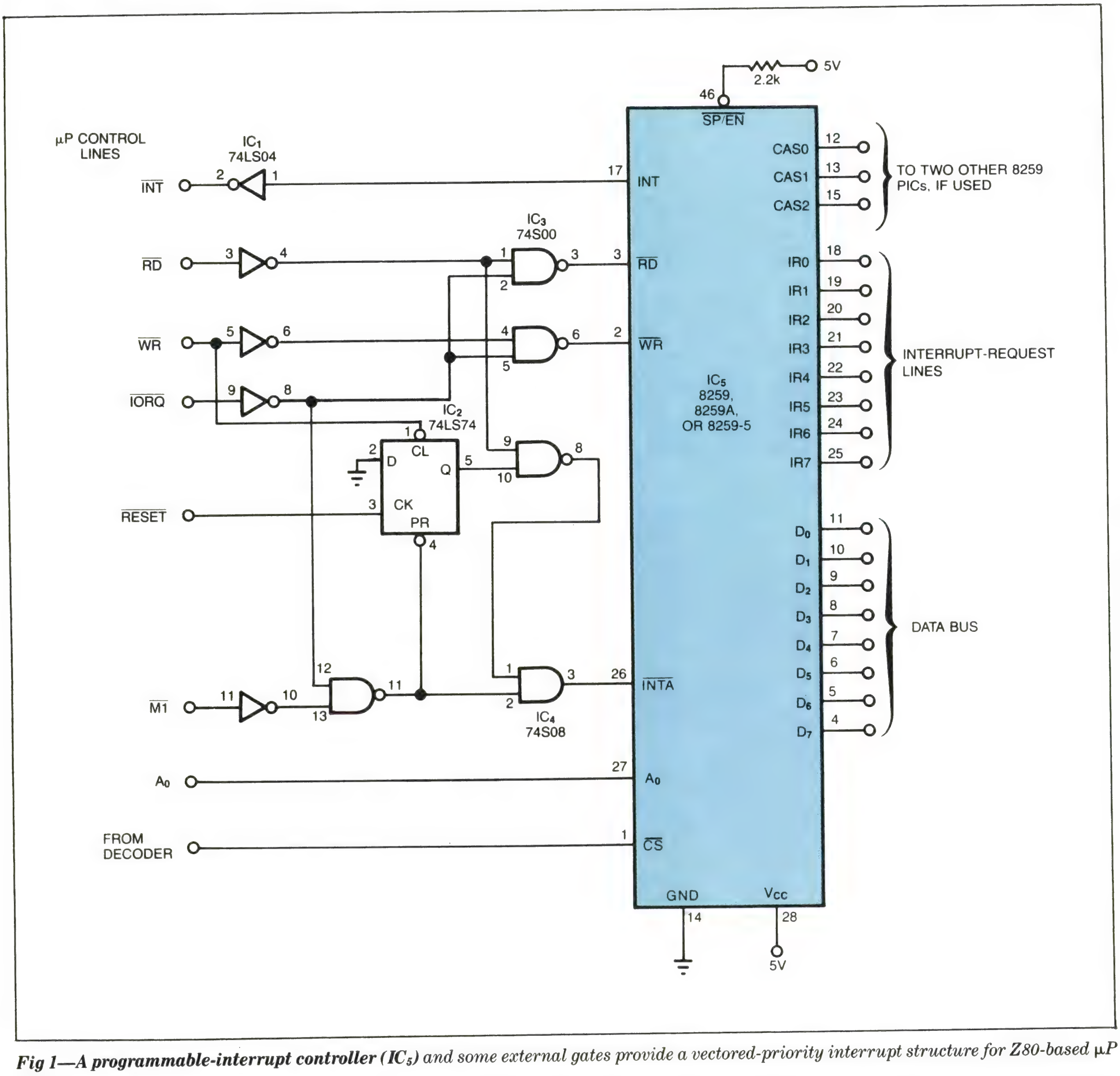

Fig 1—A programmable-interrupt controller (IC_5) and some external gates provide a vectored-priority interrupt structure for Z80-based µP systems.

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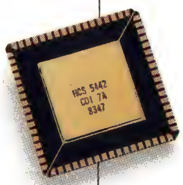

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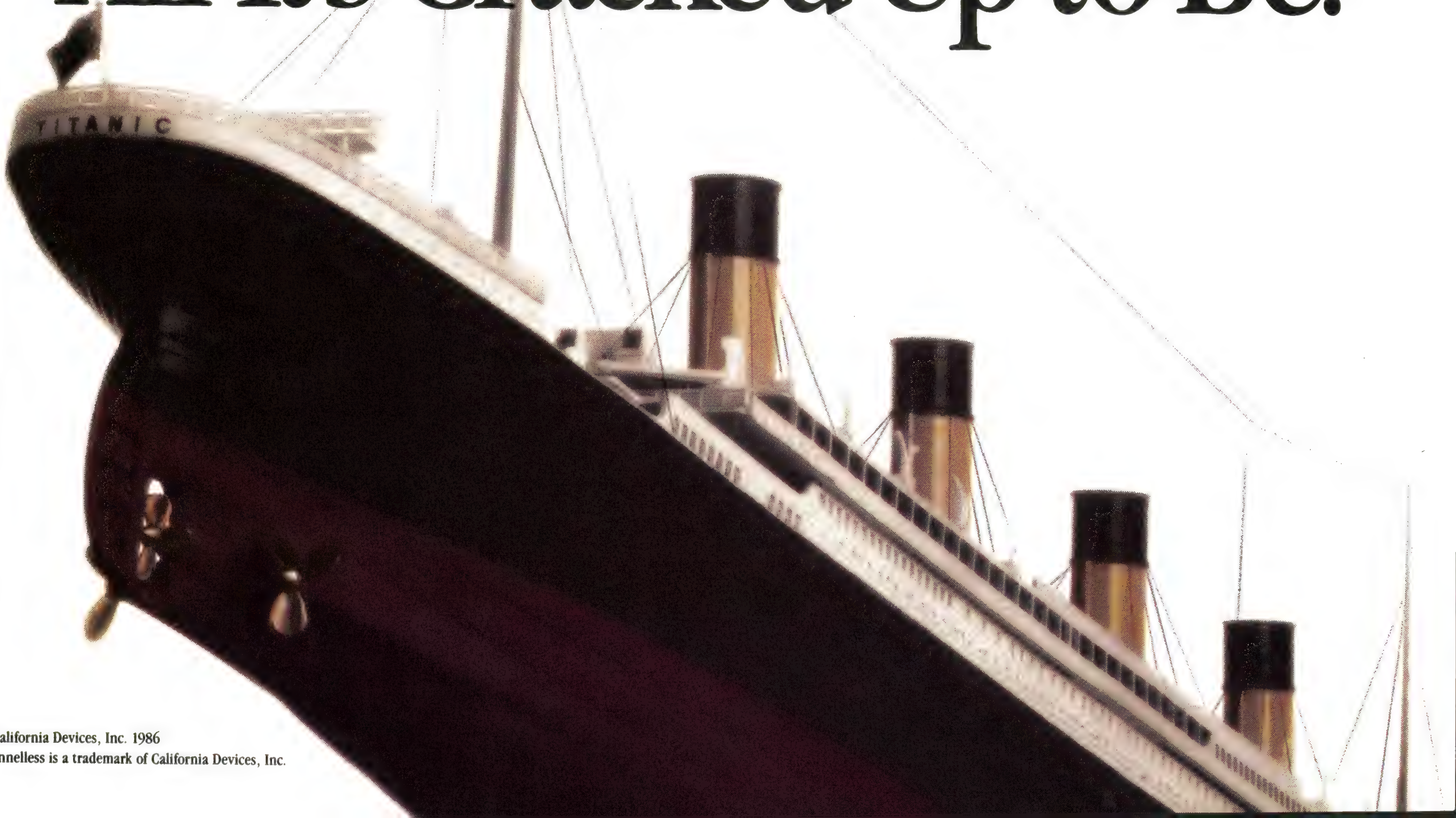

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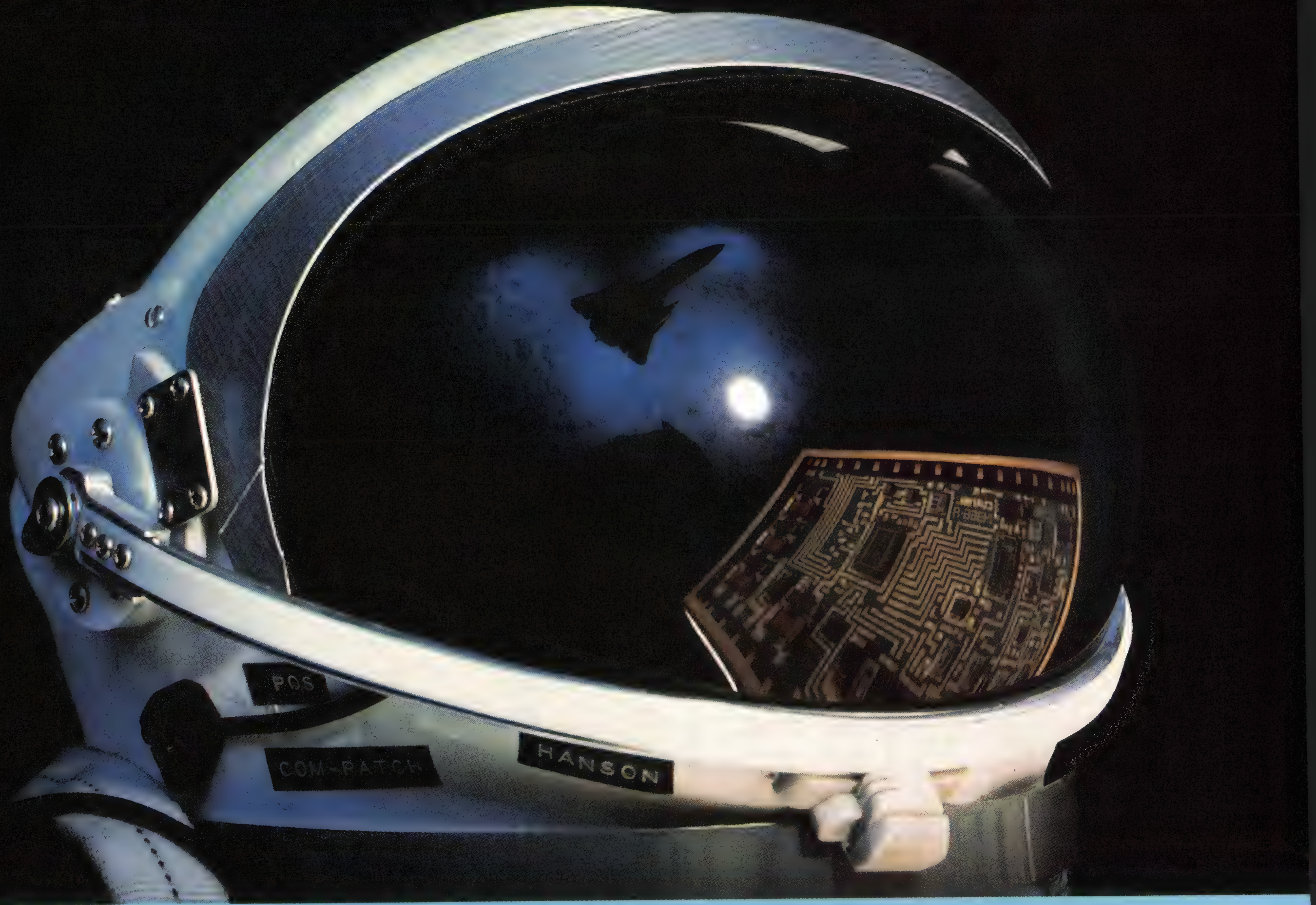

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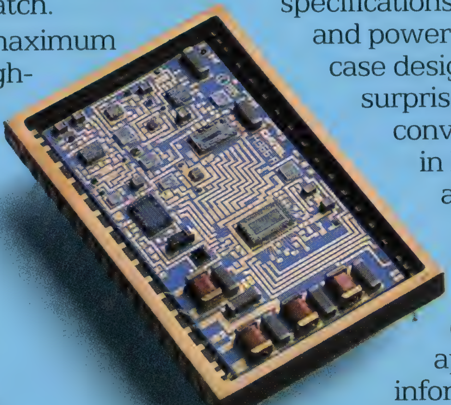

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$\overline{\text{IORQ}}$ commands generate the first $\overline{\text{INTA}}$ pulse, which places the Call op code on the data bus. Next, the μP's $\overline{\text{RD}}$ command generates the second and third $\overline{\text{INTA}}$ pulses, which causes the PIC to place upper and lower address bytes on the data bus. Flip-flop IC_2 validates these last two pulses, and then the first stack operation after the Call statement clears the flip-flop. The timing diagram (**Fig 2**) shows the overall interrupt-request/acknowledge operation. **EDN**

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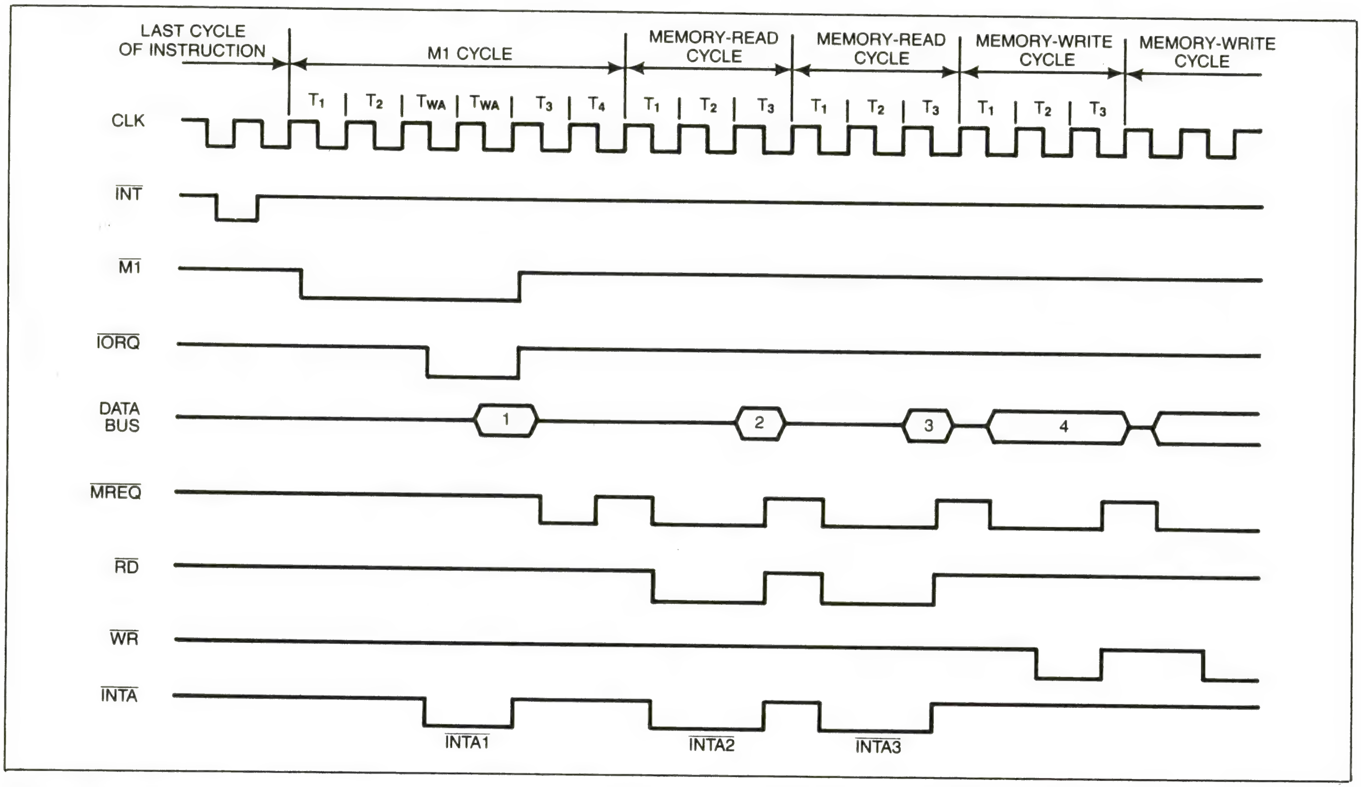

*Fig 2—**This diagram illustrates the timing relationships** for the interrupt-request/acknowledge operation in **Fig 1**.*

Subroutines handle speech companding

R Garrick and K Siil
The Logistic Software Group, Sunnyside, NY

You can use a compression subroutine (**Listing 1**) in tandem with an expansion subroutine (**Listing 2**) to increase channel bandwidth in a 68000-based speech-processing system. The compression routine takes 14-bit sign-magnitude PCM data from location IN_DAT, logarithmically compresses it, and returns 8-bit sign-exponent-mantissa data to register D0. Transmission of 8-bit data—rather than 14-bit—allows you to reduce the channel bandwidth by 43%. The expansion routine then takes 8-bit data from location COMP_DAT, transforms it back to 14-bit sign-magnitude form, and returns the expanded result to register D2.

The subroutines contain algorithms based on μ-law companding. **Fig 1** shows how these algorithms transform an 8-bit digital word to 14 bits and back. The compression routine, for example, must first mask and store the input data's sign bit. The routine then adds a bias to the input value to ensure a minimum 1 at bit position 5. The next step locates the leading 1 in the sum (which determines the exponent value) and takes the next four bits as the mantissa. Finally, the routine combines sign, exponent, and mantissa bits in an 8-bit word as shown in the flow chart (**Fig 2a**).

The simpler expansion routine first masks and stores the sign, mantissa, and exponent bits. Next, it pads the mantissa with a leading and trailing 1 and shifts the result left, according to the value of the exponent. After subtracting the original bias from this expanded

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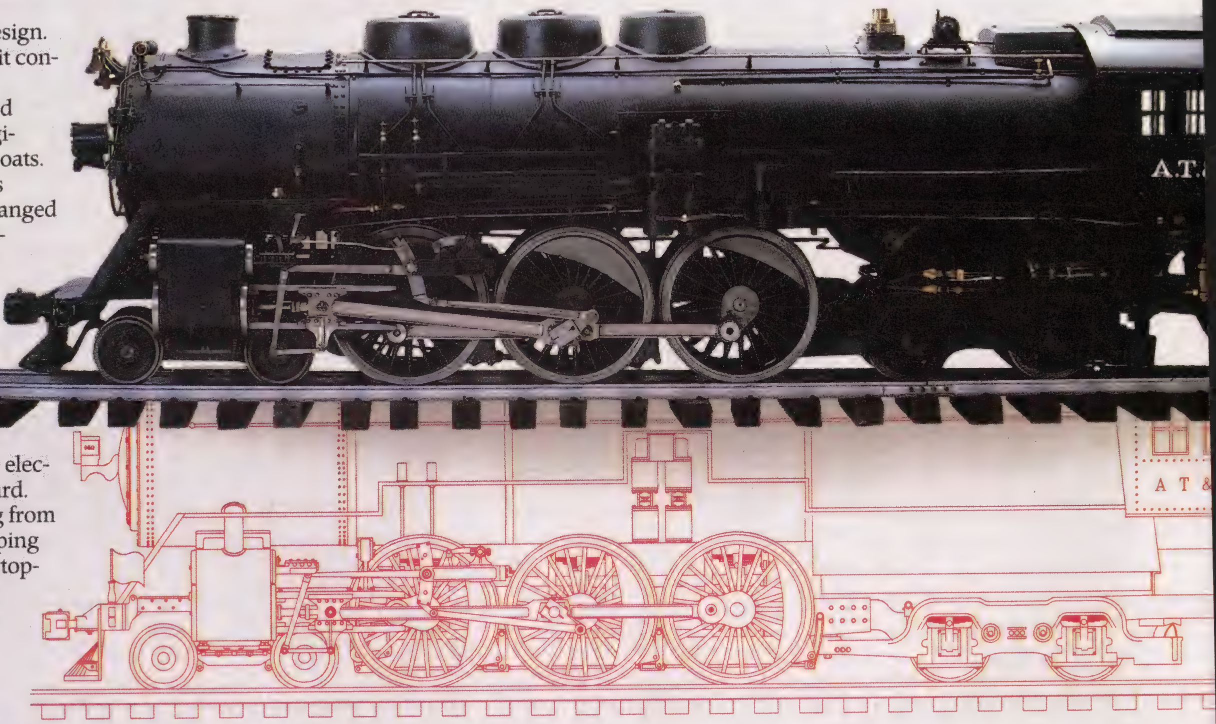

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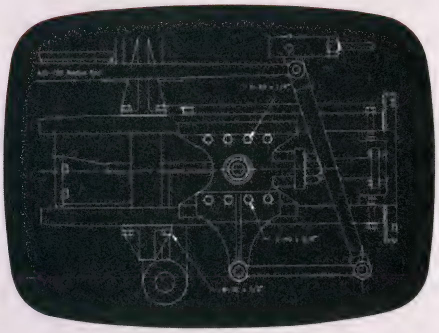

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data, the routine adds the sign bit to form a 14-bit output value. Although the algorithm only transmits a 4-bit mantissa, it achieves 5½-bit accuracy because it adds the leading 1 and because the trailing 1 represents a median value for the truncated bits.

Substituting two look-up tables for a series of lengthy

LISTING 1—µ-LAW COMPRESSION ROUTINE

```
;        REGISTER CONTENTS INITIALIZED BY EXECUTIVE
;        D4 = $1FFF         COMPLEMENT OF SIGN MASK
;        D5 = $0D           SIGN BIT LOC IN INPUT WORD
;        D6 = $2000         SIGN MASK
;        D7 = $21           BIAS
;
;  INPUT:   14 BIT SIGN-MAGNITUDE DATA AT LOCATION IN_DAT
;
;  OUTPUT:   8 BIT COMPRESSED SIGN-EXPONENT-MANTISSA DATA IN REGISTER D0
;
COMPRESS:          MOVE.W  IN_DAT,D0             ; GET DATA FOR COMPRESSION
                   MOVE.W  D0,D1                 ; COPY DATA FOR SIGN MASKING
                   AND.W   D6,D1                 ; MASK SIGN
                   LSR.W   #6,D1                 ; POSITION SIGN IN OUTPUT
                   AND.W   D4,D0                 ; STRIP SIGN FROM INPUT DATA
                   ADD.W   D7,D0                 ; ADD BIAS
                   BCLR    D5,D0                 ; OVERFLOW ?
                   BNE.S   OVERFLOW              ; YES, GO FETCH MAX EXP-MANTISSA
                   MOVE.W  D0,D2                 ; NO, MAKE COPY OF DATA
                   LSR.W   #6,D2                 ; CALCULATE TABLE OFFSET
                   MOVE.B  SHFTTBL(D2.W),D2      ; FETCH SHIFT COUNT
                   LSR.W   D2,D0                 ; SHIFT MANTISSA TO LOW FOUR BITS
                   ADD.B   EXPTABL(D2.W),D0      ; COMBINE EXP & MANTISSA
ADDSIGN:           OR.B    D1,D0                 ; ADD SIGN TO EXP-MANTISSA
                   RTS                           ; RETURN COMPRESSED DATA
OVERFLOW:          MOVEQ   #$7F,D0               ; LOAD MAXIMUM EXP-MANTISSA
                   BRA     ADDSIGN               ; GO ADD SIGN

EXPTABL:           DC.B    0                     ; EXPONENT TABLE
                   DC.B    $F0
                   DC.B    $00
                   DC.B    $10
                   DC.B    $20
                   DC.B    $30
                   DC.B    $40
                   DC.B    $50
                   DC.B    $60

SHFTTBL:           DC.B    1                     ; MANTISSA SHIFT TABLE
                   DC.B    2
                   DCB.B   2,3
                   DCB.B   4,4
                   DCB.B   8,5
                   DCB.B   16,6
                   DCB.B   32,7
                   DCB.B   64,8
```

LISTING 2—µ-LAW EXPANSION ROUTINE

```
;  INPUT:   8 BIT COMPRESSED SIGN-EXP-MANTISSA DATA AT LOCATION COMP_DAT
;
;  OUTPUT:  14 BIT EXPANDED SIGN-MAGNITUDE DATA IN REGISTER D2
;
EXPAND:            CLR.W   D0                 ; INIT OUTPUT WORD
                   MOVE.B  COMP_DAT,D0        ; GET COMPRESSED DATA
                   MOVE.W  D0,D1              ; COPY DATA FOR SIGN EXTRACTION
                   ANDI.W  #$80,D1            ; MASK AND STORE SIGN
                   LSL.W   #6,D1              ; POSITION SIGN IN OUTPUT
                   MOVE.W  D0,D2              ; COPY INPUT FOR MANTISSA MASKING
                   ANDI.W  #$0F,D2            ; MASK AND STORE MANTISSA
                   LSL.W   #1,D2              ; PREPARE MANTISSA FOR PACKING W/ 1'S
                   ORI.W   #$21,D2            ; ADD LEADING AND TRAILING 1'S
                   ANDI.W  #$70,D0            ; MASK EXPONENT
                   LSR.W   #4,D0              ; RIGHT JUSTIFY EXPONENT
                   LSL.W   D0,D2              ; EXPONENTIATE MANTISSA
                   SUB.W   #33,D2             ; REMOVE BIAS
                   OR.W    D1,D2              ; ADD SIGN TO EXPANDED DATA
                   RTS                        ; RETURN EXPANDED DATA
```

linear or binary bit searches speeds execution of the compression routine by returning values for the leading 1 and the exponent. The compression subroutine requires 156 clock cycles; the expansion subroutine requires an additional 144 cycles. Thus, operating the 68000 with a 12.5-MHz clock and a tight executive-program loop provides ample bandwidth for one processor to handle full-duplex voice communications.

EDN

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BIASED COMPRESSION (ENCODING) TABLE

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	X	S	0	0	0	0	0	0	0	1	M_3	M_2	M_1	M_0	X	S	0	0	0	M_3	M_2	M_1	M_0
X	X	S	0	0	0	0	0	0	1	M_3	M_2	M_1	M_0	X	X	S	0	0	1	M_3	M_2	M_1	M_0
X	X	S	0	0	0	0	0	1	M_3	M_2	M_1	M_0	X	X	X	S	0	1	0	M_3	M_2	M_1	M_0
X	X	S	0	0	0	0	1	M_3	M_2	M_1	M_0	X	X	X	X	S	0	1	1	M_3	M_2	M_1	M_0
X	X	S	0	0	0	1	M_3	M_2	M_1	M_0	X	X	X	X	X	S	1	0	0	M_3	M_2	M_1	M_0
X	X	S	0	0	1	M_3	M_2	M_1	M_0	X	X	X	X	X	X	S	1	0	1	M_3	M_2	M_1	M_0
X	X	S	0	1	M_3	M_2	M_1	M_0	X	X	X	X	X	X		S	1	1	0	M_3	M_2	M_1	M_0
X	X	S	1	M_3	M_2	M_1	M_0	X	X	X	X	X	X	X	X	S	1	1	1	M_3	M_2	M_1	M_0

BIASED EXPANSION (DECODING) TABLE

7	6	5	4	3	2	1	0	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
S	0	0	0	M_3	M_2	M_1	M_0	X	X	S	0	0	0	0	0	0	0	1	M_3	M_2	M_1	M_0	1
S	0	0	1	M_3	M_2	M_1	M_0	X	X	S	0	0	0	0	0	0	1	M_3	M_2	M_1	M_0	1	0
S	0	1	0	M_3	M_2	M_1	M_0	X	X	S	0	0	0	0	0	1	M_3	M_2	M_1	M_0	1	0	0
S	0	1	1	M_3	M_2	M_1	M_0	X	X	S	0	0	0	0	1	M_3	M_2	M_1	M_0	1	0	0	0
S	1	0	0	M_3	M_2	M_1	M_0	X	X	S	0	0	0	1	M_3	M_2	M_1	M_0	1	0	0	0	0
S	1	0	1	M_3	M_2	M_1	M_0	X	X	S	0	0	1	M_3	M_2	M_1	M_0	1	0	0	0	0	0
S	1	1	0	M_3	M_2	M_1	M_0	X	X	S	0	1	M_3	M_2	M_1	M_0	1	0	0	0	0	0	
S	1	1	1	M_3	M_2	M_1	M_0	X	X	S	1	M_3	M_2	M_1	M_0	1	0	0	0	0	0	0	0

*Fig 1—**These encoding and decoding tables** show the result of the subroutine operations in **Listing 1** and **Listing 2**.*

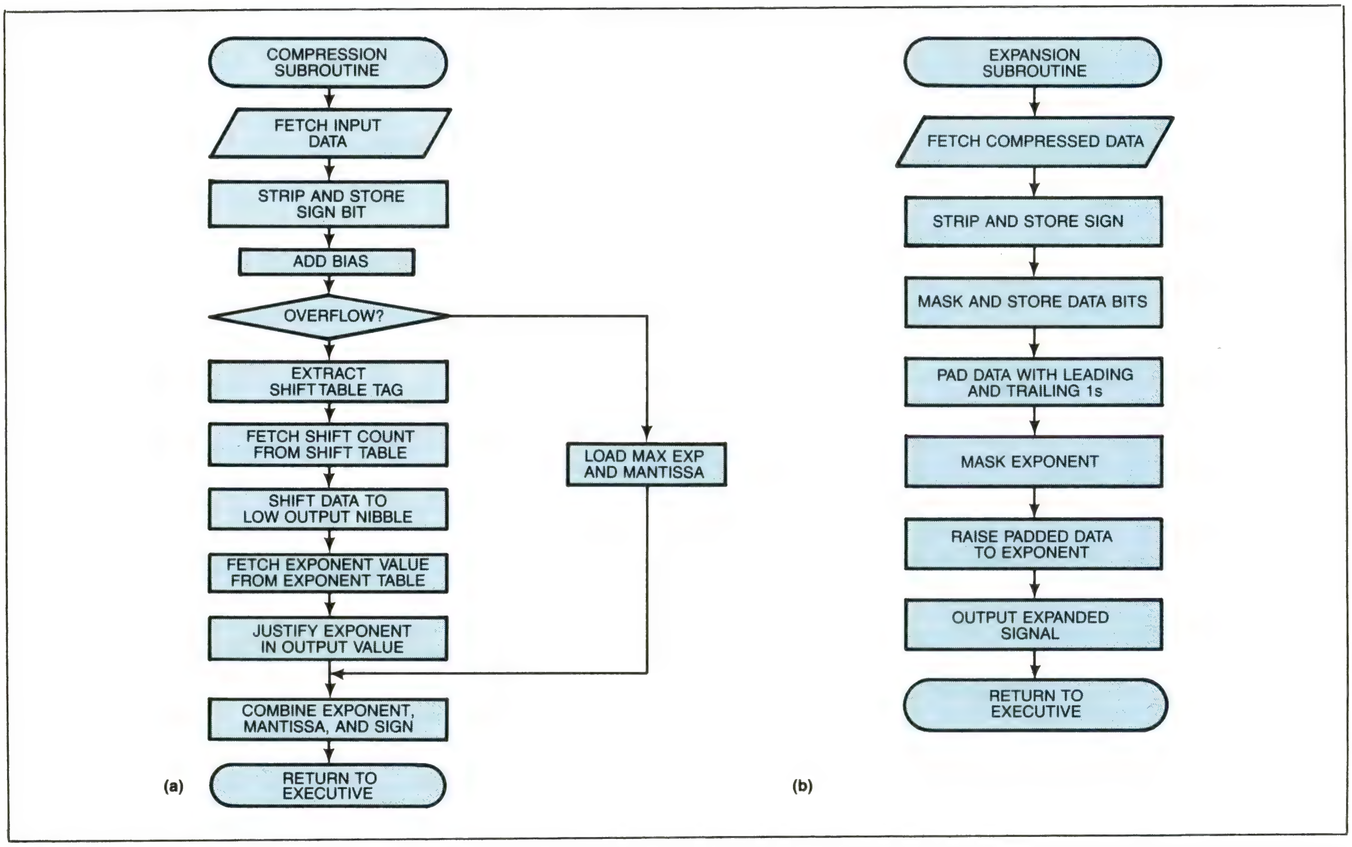

*Fig 2—**One flow chart (a) illustrates** the algorithm for **Listing 1**'s compression subroutine, and the other **(b)** shows **Listing 2**'s expansion subroutine.*

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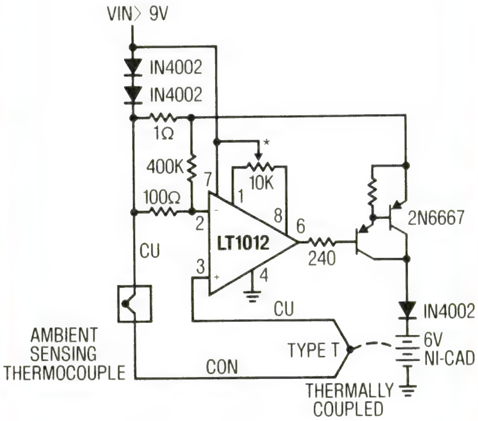

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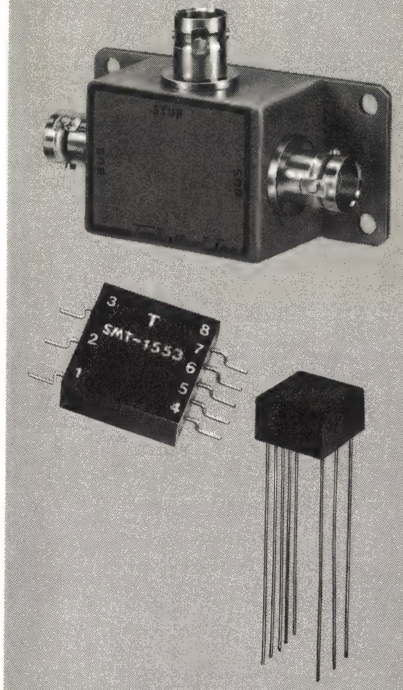
Mil-Std 1553 data bus couplers, interface transformers, absolutely to spec.



Just paying the price for 1553-rated components doesn't guarantee their ability to perform.

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CIRCLE NO 110

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We are volume producers of industry standard gate array families such as our high performance 2µ devices, the 17G series. It has a 1.5 nanosecond gate speed with up to 10,000 gates as well as a macro library of 7400 type SSI/MSI functions. These units have fully compatible TTL/CMOS input and output and can be configured with up to 232 available pins. Our 3µ industry standard CMOS gate array family, the 15G, has a 2.5 nanosecond gate speed with up to 6000 gates available. In fact, that's why these industry standard families are second-sourced with LSI Logic Corporation.

And we're working now on the next generation of CMOS gate arrays as well as full standard cell capability to be introduced shortly.

TOSHIBA IS PRODUCTION POWER

Toshiba is the world's largest producer of high quality CMOS devices, and one of the few companies with high volume production experience and capability in CMOS gate arrays.

All this means Toshiba can provide the design support you need with a volume production capability to assure that your designs become delivered product in the right quantities on time.

So if you are planning a 2µ gate array design, plan with the people who have the power. Plan with Toshiba.

Part Number	Array Size	Max Pins		Gate Length	Gate Delay (ns) [1]	
					TYP	MAX [2]
TC15G008	880		74	3	2.5	5.0
TC15G014	1400		92	3	2.5	5.0
TC15G022	2200		114	3	2.5	5.0
TC15G032	3200		138	3	2.5	5.0
TC15G042	4200		156	3	2.5	5.0
TC15G060	6000		180	3	2.5	5.0
TC17G005	540	44	48	2	1.5	3.0
TC17G008	880	52	68	2	1.5	3.0
TC17G014	1400	68	86	2	1.5	3.0
TC17G022	2200	82	106	2	1.5	3.0
TC17G032	3200	98	128	2	1.5	3.0
TC17G042	4200	118	150	2	1.5	3.0
TC17G060	6000	146	188	2	1.5	3.0
TC17G080	8000	174	222	2	1.5	3.0
TC17G100	10000	180	232	2	1.5	3.0

NOTES:
[1] For a 2 input NAND gate having a fan out of 2 and 2mm of metal interconnect.
[2] At 70°C and Vdd = 5v ± 5%

TOSHIBA. THE POWER IN GATE ARRAYS.

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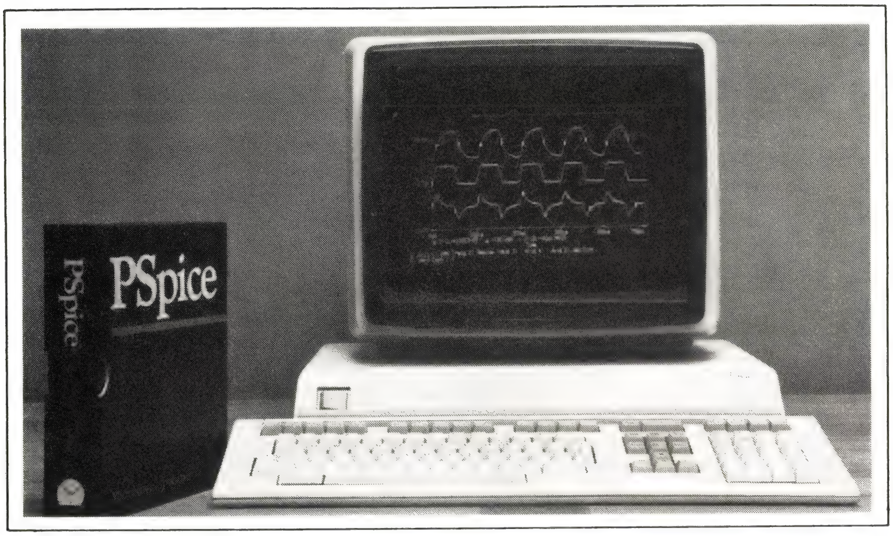
CIRCLE NO 46

NEW PRODUCTS

COMPUTER-AIDED ENGINEERING



VAX-BASED SPICE

- *Circuit simulator*
- *Runs on all VAX computers*

The PSpice analog-circuit simulator runs on members of the DEC VAX family, including the MicroVAX II. The program's Device Equations option, Probe graphics postprocessor, and Parts parameter estimator also run on the VAX. Both Probe and Parts can display graphics on DEC VT125 and VT200 and on Tektronix 4014 terminals. The programs can also generate output files for dot-matrix printers and pen plotters. VAX-based versions of these programs use the same input syntax and give the same results as the PC-based versions do. PSpice, \$1900; Device Equations, \$730; Probe, \$900; Parts, \$900.

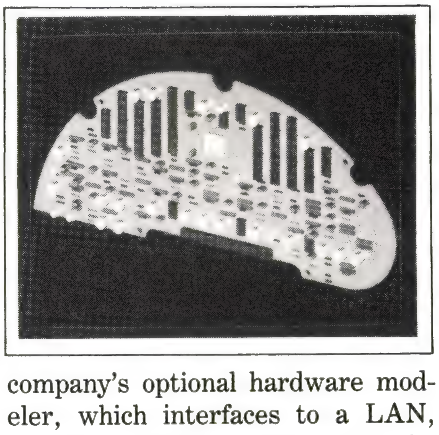
MicroSim Corp, 23175 La Cadena Dr, Laguna Hills, CA 92653. Phone (714) 770-3022.

Circle No 363

CAE SOFTWARE

- *Design capture and analysis*
- *Runs on VAX-based computers*

The Bravo 3 line of CAE software includes schematic-capture, design-analysis, and layout tools. The software assists you in designing both pc boards and VLSI devices. The company's schematic editor includes a component library; you can search for devices in the library by name or by description. The package supports multiple levels of design hierarchy. Bravo 3's logic-analysis program integrates logic, timing, and fault simulation. It lets you simulate designs at gate, functional, and behavioral levels, and it includes more than 100 primitive elements. The company's optional hardware modeler, which interfaces to a LAN, simulates VLSI components. The pc-board layout software comprises automatic and interactive tools. The automatic-layout tools include schematic analysis, gate packaging, placement, routing, and design verification. The automatic-placement feature includes packaged or gate-level input, preplacement, horizontal or vertical weighting, and back annotation. The company's autorouter can perform multilayer, diagonal, memory-array, pin-swapping, and power/ground routing. The software line's VLSI engineering tools offer design- and electrical-rule checking, mask formatting for optical-pattern generation, and layout-versus-logic consistency checks. The analysis and layout products run on VAX-based computers. The schematic editor runs on VAX computers, as well as on this company's Sun-based 4670 graphics terminal. Graphics terminal, schematic editor, drafting, and TTL-device simulation library, \$29,000.



Applicon, 4251 Plymouth Rd, Ann Arbor, MI 48106. Phone (313) 995-6000.

Circle No 364

DESIGN/TEST LINK

- *Links Daisy systems to VLSI test systems*
- *Translates control programs*

The Daisy-to-GenRad interface, which links Daisy design workstations with this company's VLSI test systems, translates Daisy simulation data into the company's test vector format. The program also translates portions of the test system's control program. Debug data from the interface package helps you modify your simulation vectors to meet the tester's requirements. The program runs on Daisy's Logician and Megalogician workstations and interfaces to this company's GR160 and GR180 VLSI test systems. Single license, \$10,000; site license, \$20,000.

GenRad Inc, 510 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 263-1000.

Circle No 365

We put fundamentals together in new ways to make things remarkably better.

We compared apples and oranges in a brand new way, to create a better power supply.

For two years, our R&D engineers reviewed everything known about the technology and use of high-power, phase-controlled, dc power supplies, to learn how to make one that would better suit all your applications.

We discovered that many accepted engineering fundamentals needed to be rearranged to improve performance.

The result is our new DCR-T Series. 3-phase input, regulated dc high-power supplies, with unique power ranges that save you money, and performance features simply not available elsewhere. Includes resistive and voltage remote programming of V, I and OVP, and compatibility with Sorensen IEEE programmers. Remote inhibit, OVP shutdown, and current drives for remote meters and all panel indicators are standard. There's even a circuit that senses open remote programming lines and prevents the product under burn-in from becoming a burn-out.

There will be nine 10-kW models of the DCR-T, from 0-8 Vdc to 0-600 Vdc and 16 Adc to 900 Adc. Comparing them with other power supplies is harder than comparing apples and oranges, because the DCR-T is a whole new form of life.

MODEL	Voltage (Vdc)	Current (Adc @ 50° C)
DCR 8-900T	0-8	900
DCR 16-625T	0-16	625
DCR 32-310T	0-32	310
DCR 55-180T	0-55	180
DCR 80-125T	0-80	125
DCR 110-90T	0-110	90
DCR 160-62T	0-160	62
DCR 300-33T	0-300	33
DCR 600-16T	0-600	16

Manufacturer's Suggested List Price $3,900.

For more information contact:
Sorensen Company, 676 Island Pond Road
Manchester, NH 03103 USA (603) 668-4500

Sorensen
A **Raytheon** Company

CIRCLE NO 111

GATE-ARRAY DESIGN

- *For Mentor Graphics' workstations*
- *Improves simulation of bipolar gate arrays*

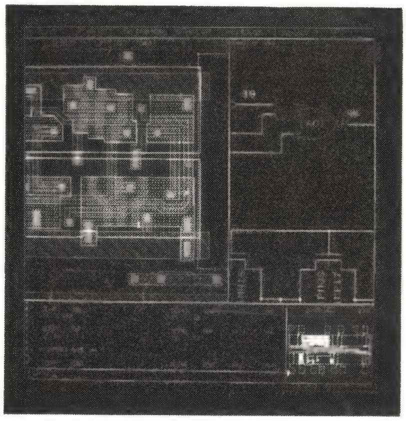
The Software Toolkit, which provides an interface to Mentor Graphics' Idea 1000 workstations, improves the simulation of this company's bipolar gate arrays. The package generates models of Series HE2000, HM3500, and HE8000 gate arrays. The kit consists of two programs, Stats and Delay; a macrocell library; and a product-specific technology table. Stats detects technology-dependent design errors. It reports device loads, power dissipation, cell count, cell utilization, and preplacement and layout statistics. Delay uses load factors, junction temperatures, and wire capacitances to calculate propagation delays. You can run the program both before and after routing in order to compare the propagation delays calculated for estimated and actual wire lengths. Both programs use a technology table that contains product-specific propagation delays, loading parameters, and electrical characteristics. The kit includes a library of 150 macrocells. The program is available on floppy disks and on magnetic tape. $25,000.

Honeywell Inc, Digital Product Center, 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906. Phone (800) 328-5111, ext 3422.

Circle No 366

IC-LAYOUT VERIFIER

- *Schematic-to-layout debugging module*
- *Edits, detects, and corrects errors*



Remedi, a schematic-to-layout debugging module, operates in conjunction with this company's Chipgraph custom-VLSI layout editor and ECAD's Dracula II layout-verification package. This program integrates net lists and physical layouts and displays inconsistencies between schematics and layouts in windows on a workstation, thus helping you see discrepancies between your layout and your schematic. Using the program, you can edit, detect, and correct layout errors without exiting your layout edi-

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If your design includes an 80C31 system, EDI's all CMOS μPak provides a space-saving
pin to pin compatible to the 80C31, the μPak is a low power, space-saving powerhouse.
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Electronic Designs Europe, Shelley House, The Avenue, Lightwater, Surrey GUI8 5RF, U.K., Telephone 0276 72637, TELEX 85832

tor. The software is compatible with all IC-design hierarchies and methodologies. $14,900.

Mentor Graphics Corp, 8500 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 626-7000.

Circle No 367

FILTER DESIGN

- *For all active filters*
- *Runs on the IBM PC*

You can use Filter to design active filters on an IBM PC or compatible computer. The program can design Butterworth, Chebyshev, inverse Chebyshev, and all pass filters to the thirtieth order. It can also aid in the design of lowpass, highpass, bandpass, and bandstop filters at any frequency. The program produces Bode plots of filters and calculates group delays. It also lists the transfer function of each filter. You can factor the transfer function into linear and quadratic parts and display the Q of each of these factors. The package creates an output file that you can transfer to LSAP, the company's linear-systems program. The software requires a PC with 256k bytes of memory, any graphics adapter, and either a floppy or a hard disk. The program is compatible with the 8087 math coprocessor, but does not require one. $750.

California Software Systems, 25642 Hazelnut Lane, El Toro, CA 92630. Phone (714) 581-7654.

Circle No 368

SCHEMATIC EDITOR

- *Features symbol rotation*
- *Comes with standard libraries*

The Dash 4 schematic designer features an expanded data management capability that lets you hide over 4000 characters in one field. This capability thus allows you to include information specific to a particular translator or other postprocessor as an integral part of the schematic, without increasing the size of the symbols on the schematic. You can use a text editor to modify the hidden text. Other features of the schematic editor are symbol rotation and mirror imaging. For representations of elements like buses, the editor lets you create curved and angled lines. This feature permits you to satisfy MIL-D 1000 specs; a library of MIL-D 1000 components is available as an option. The schematic editor offers centered, right-hand, or left-hand justified text. You can create text in any of seven fonts; eight line types, such as dotted and solid lines, are available. The package comes with a set of standard libraries that include CMOS, discrete, ECL, memory, TTL, and IEEE, as well as Intel and Motorola libraries. Gould/AMI and MIL-D-1000 libraries are op-

all Wonder.

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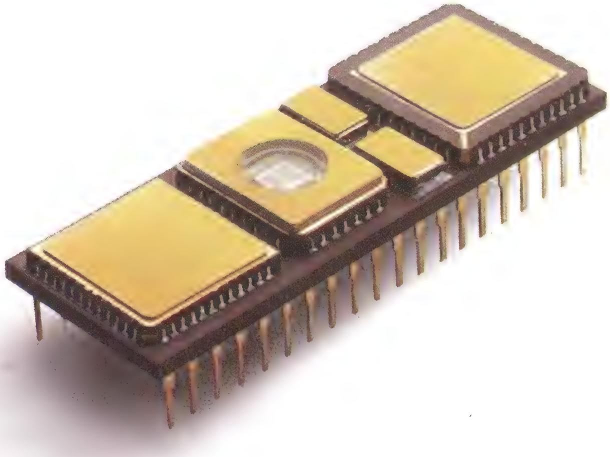
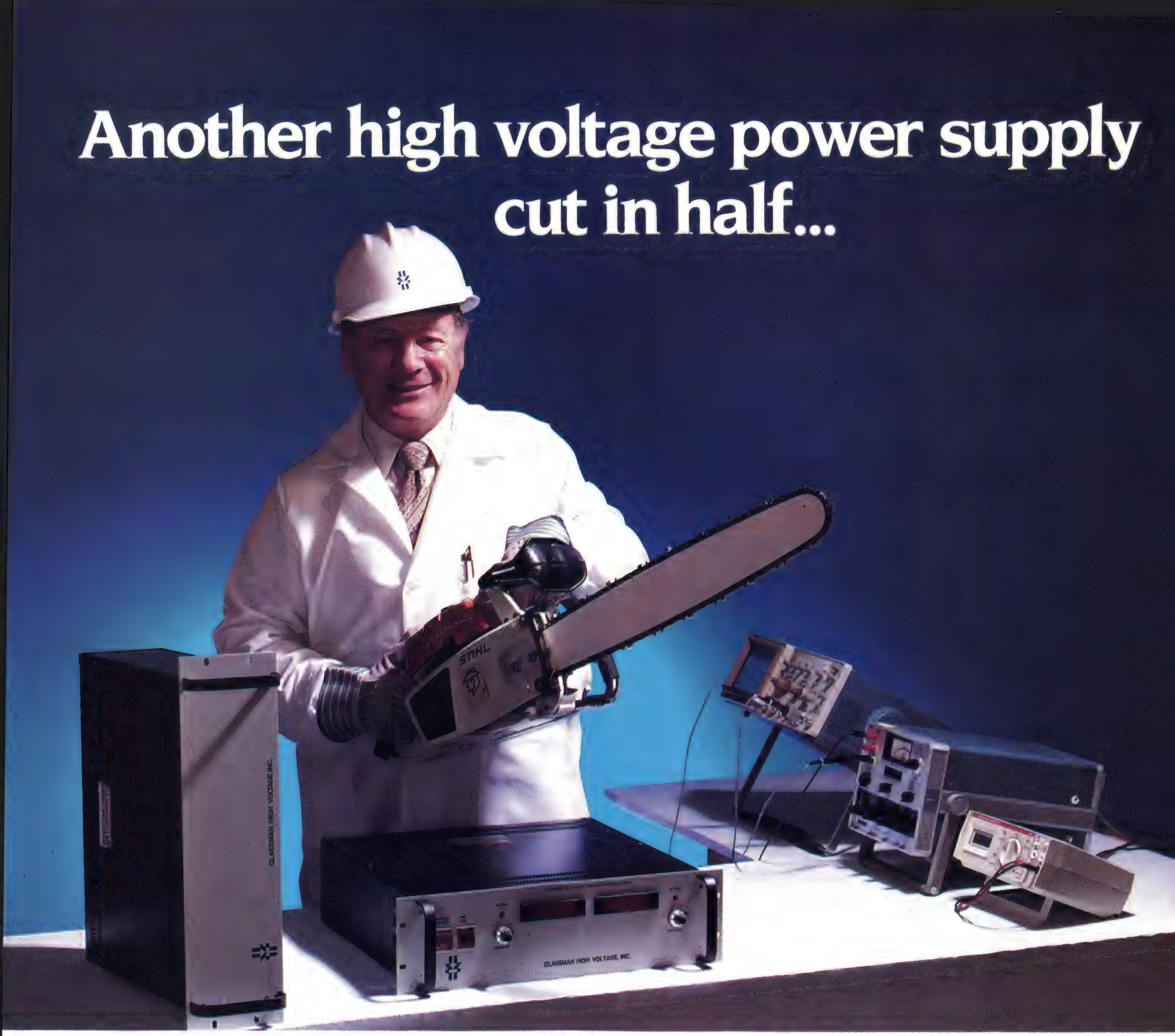
vailable for Military, Industrial and Commercial applications in 8 and 12 MHz



EDI
The future . . . today.

CIRCLE NO 112

Another high voltage power supply cut in half...



The WH Series...500 watts, 1/2 the space, 1/2 the weight, and we even cut the price!

When Glassman packed 500 Watts @ 80kV into 10 1/2" of rack space a few years ago, it was a pretty impressive feat.

Although that may seem commonplace today, the next step, which we've just taken,isn't. We've packed 500 watts @ up to 75kV in half that space...5 1/4". The WH Series is one half the size and weight of the PG Series models it replaces. In it, you get more regulated high voltage in less space than any other supply we know of.

To accomplish this, we've developed some new circuitry that we believe has increased the reliability of our already sound, field proven switch-mode technology.

If light weight, compactness, tight regulation, and high reliability are major factors in your high voltage power supply requirements, then call John Belden at 201-534-9007 for complete details on the new WH Series.

Innovations in high voltage power supply technology.

GLASSMAN HIGH VOLTAGE INC.
Route #22 (East), Salem Industrial Park, P.O. Box 551, Whitehouse Station, N.J. 08889
(201) 534-9007 • TWX 710-480-2839
CIRCLE NO 113

tional. The user's manual is built into the software. The package runs on an IBM PC that has 512k bytes of RAM, DOS 2.0 or higher, and a hard disk. $5980; MIL-D-1000 library, $200.

FutureNet, 9310 Topanga Canyon Blvd, Chatsworth, CA 91311. Phone (818) 700-0691. TWX 910-494-2681.

Circle No 369

CIRCUIT SIMULATOR

- *Offers transient analysis*
- *Runs on IBM PCs*

The EC-Ace circuit simulator features ac- and dc-transient analysis capabilities and nonlinear transfer functions. It is a stripped-down version of the vendors's ECA 2.2 simulator. The interactive simulator provides graphics output and editing capabilities. The package includes a 200-pg user's manual. You can run this circuit simulator on IBM PCs (including PCjr) and compatibles, Tandy 1000, Zenith 150, and Leading Edge computers. You can upgrade the program to ECA 2.2 within 12 months of purchase. EC-Ace, $95; ECA 2.2, $450.

Tatum Labs, 33 Main St, Newtown, CT 06470. Phone (203) 426-2184.

Circle No 370

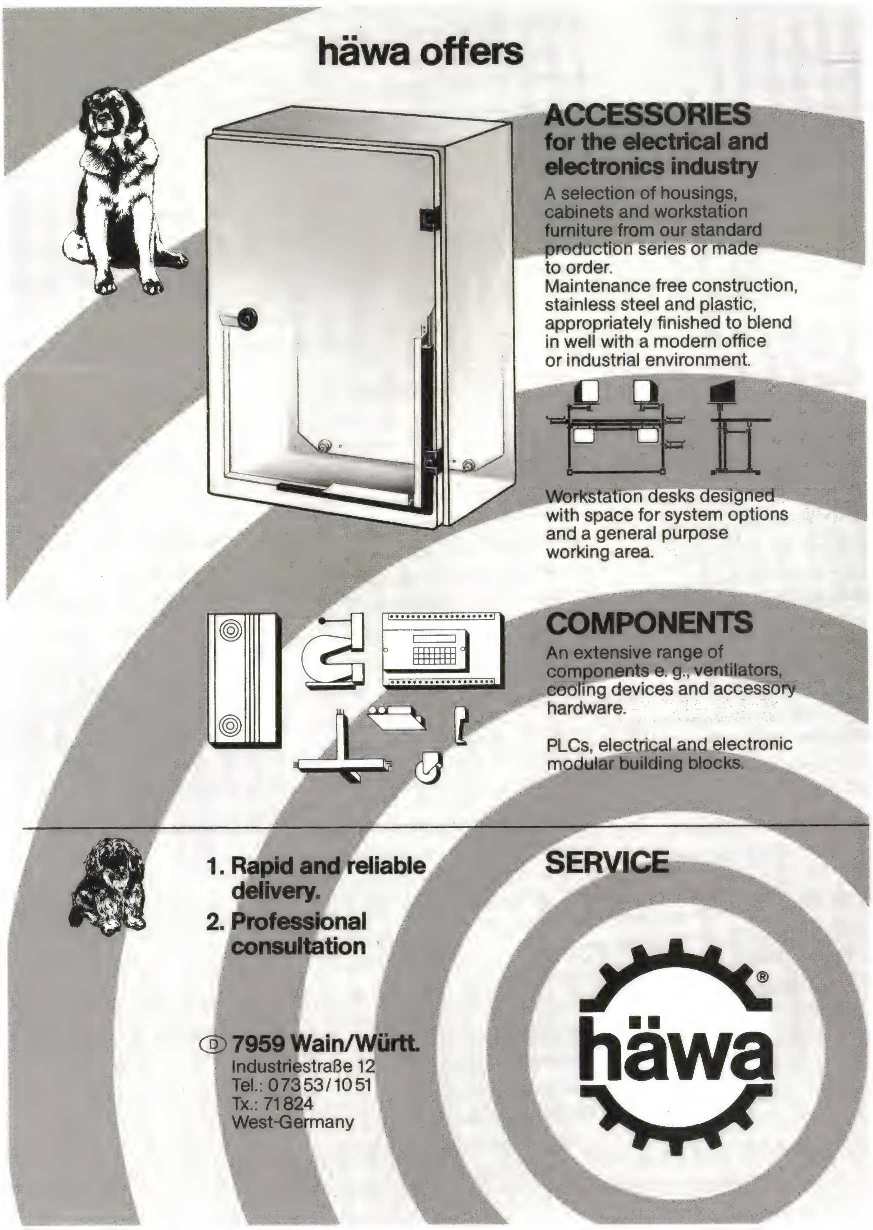
POWER-SUPPLY CAE

- *Simulates transformer cores*
- *Offers power-device library*

This option for the company's Analog Workbench CAE software, the Power Design Module, enables you to predict the behavior of transformer cores. Based on Spice Plus (the company's enhanced version of the Spice 3 circuit simulator), the power-design package consists of a magnetics model that simulates the nonlinear characteristics of transformer-core materials, a core-materials library that lets you specify transformer-core and magnetic properties, and a power-device library. The magnetics model defines both major and minor hysteresis loops. The power-device library contains ICs, such as pulse-width modulators (eg the UC1525), current-mode controllers (eg the UC1846), diodes, and bipolar transistors. Transistor models incorporate parasitic effects. The option runs on workstations from Sun Microsystems, Apollo, and Hewlett-Packard workstations as well as on the IBM PC/AT-based PC Workbench. Workstation-based versions, $7500; PC/AT-based version, $5000.

Analog Design Tools Inc, 66 Willow Pl, Menlo Park, CA 94025. Phone (415) 328-0780.

Circle No 371



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CIRCLE NO 114

NEW PRODUCTS

COMPUTERS & PERIPHERALS

RASTER PROCESSOR

- *Relieves host computer of rasterization*
- *Features a 32-bit μP*

When running CAE applications, you can use the Model 810 Raster Processing Machine (RPM) to relieve your host computer of the rasterization process. The machine contains a 32-bit μP and 2M bytes of memory. It is suitable for use with plots of low to medium complexity. The unit offers no upgrade capability, however. $7950 (OEM qty).

Versatec, 2710 Walsh Ave, Santa Clara, CA 95051. Phone (800) 538-6477; in CA, (800) 341-6060. TWX 910-338-0243.

Circle No 372

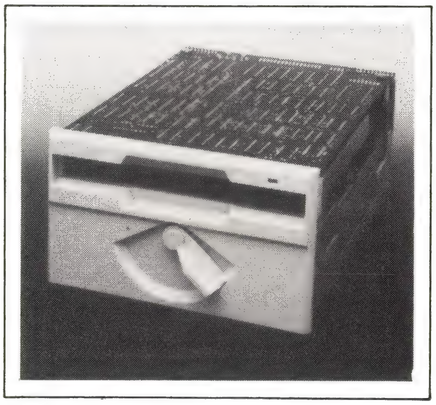
PC/AT COMPATIBLE

- *Includes 220W power supply*
- *CPU can run at 6 or 8 MHz*

The A*Star is an IBM PC/AT-compatible computer that includes a 220W power supply, a 1.2M-byte floppy-disk drive, 512k bytes of RAM, a hard- and floppy-disk drive controller located on the computer's mother board, a tactile-feedback keyboard, multiuser network circuitry, and a clock/calendar with battery backup. You can run its 80286 CPU at 6 or 8 MHz either by flipping a switch located at the back of the computer or by using a software command. Optional accessories include a 20M-byte hard-disk drive, a 12-in. monochrome display monitor with 720×350-pixel resolution, and a memory-expansion kit that extends the computer's RAM to 1M byte. An array of network accessories is also available, including a data booster, coax connectors and cables, and network adapters for other manufacturers' IBM compatibles. The unit comes with a 31-day money-back guarantee. $1495; 20M-byte disk drive, $449; 12-in. display, $139; memory kit, $95.

Wells American Corp, 3243 Sunset Blvd, West Columbia, SC 29169. Phone (803) 796-7800. TWX 510-601-2645.

Circle No 373



SCSI OPTICAL DRIVE

- *Features 4M bytes of storage*
- *Transfers data at 2M bps*

Providing 200M bytes of storage area on each side of a removable, write-once optical disk, the SCSI 5984 disk drive also supports the entire Small Computer Systems Interface (SCSI) Common Command Set. This characteristic allows you to use existing driver codes as a foundation for specific applications, thus reducing system-development time. Features include 1:1 interleaving, multitrack buffering, a data-transfer rate of 2.2M bps, and a 195-msec average access time. The unit contains a proprietary error-correction-code (ECC) chip that can correct as many as 24 bad bytes per sector while using 9.4% overhead. To facilitate data transfer between incompatible computers, this SCSI storage system can read and write optical-disk cartridges used in any of the manufacturer's other 5¼-in. optical drive systems. You can connect as many as four drives to a single controller. A SCSI 5984 system evaluation kit, including a drive, controller, optical-disk cartridge, and software tools costs $5000. Drives, $975 to $3400; controllers, $350 to $650 (both OEM qty).

Optotech Inc, 770 Wooten Rd, Suite 109, Colorado Springs, CO 80915. Phone (303) 570-7500. TLX 592966.

Circle No 374

Fujitsu's line of compatible SCSI data storage products will help you drive your system to its full performance potential.

If you want cartridge tape drives, 5¼-inch, 8-inch, and 10½-inch Winchester drives — or any combination thereof — on your SCSI bus, you'll never miss with Fujitsu America.

Our SCSI storage systems and products can keep up with the most sophisticated multi-host, multi-tasking SCSI-based system you can design. You can take full advantage of the extended performance features of SCSI — with products that set performance standards of their own.

Our M1053 Series Intelligent Disk Controller (IDC) can be configured with up to four drives on a single node, for a storage capacity that can exceed 2.7 Gigabytes. Choose our 8-inch, 337 MB drives or our 10½-inch Eagle XP, 689 MB drives. The M1053 offers either single-ended or differential drivers and common command set support for easy integration into any SCSI environment.

For 5¼-inch drives, there's the M1054 IDC. With up to four Fujitsu 172 MB, 5¼-inch drives on this controller, you can get large capacity and high performance in a compact package.

And Fujitsu's SCSI family even meets your need for cost-effective back-up devices. Our 125 MB, ½-inch cartridge tape drive provides a unique solution to your SCSI tape requirements.

If you'd like to put your SCSI system into high gear — stop! And find out more about Fujitsu's compatible data storage products. Call (408) 946-8777. Or write Fujitsu America, Inc., Storage Products Division, 3055 Orchard Drive, San Jose, CA 95134-2017.

Put Fujitsu drives on your SCSI bus. And give superior system performance the green light.

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CIRCLE NO 115

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FILM RECORDER

- *Produces slides or prints of computer graphics*
- *Uses Ektachrome, Polachrome, or Polacolor ER film*

Providing internal vector-to-raster processing, the Turbograph 2100 translates graphics data from your host computer system and records the data as images on photographic film, allowing you to make slides or prints of your computer-generated graphics. You can connect the Turbograph to your host computer via an RS-232C interface. A digital controller in the recorder then converts the computer image into a 2048×2048-pixel raster format and sends the rasterized image to a digital film recorder. The unit uses Kodak Ektachrome, Polaroid Polachrome, and Polaroid Polacolor ER film. $6995. Delivery, 60 to 90 days ARO.

AMF Logic Sciences Inc, 10808 Fallstone Rd, Houston, TX 77099. Phone (713) 879-0536.

Circle No 375

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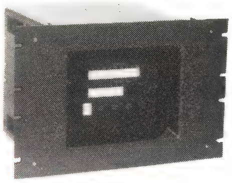
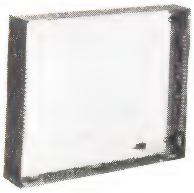
At EMS, the quality and reliability of our TOUCH products is achieved at a low cost.

Desktop TID



Rack-mount TID



Custom Touch Panel

Coming Soon: Color Touch and Flat TID

The **Touch Information Display** (TID) functions as a standard ASCII terminal or PC compatible monitor. Both are available in a rugged metal desktop or rack-mount housing, suitable for both public and industrial environments.

The 12" monochrome **TID Terminal** and **Monitor** communicate through an RS-232 or optional RS-422 port. (Monitor accepts RS-170 composite video input) With the Terminal, an optional feature is 16 pages of downloadable display memory.

Customized touch panels are available for OEM applications.

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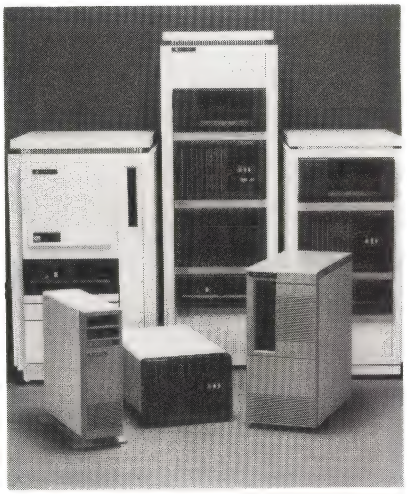
CIRCLE NO 116

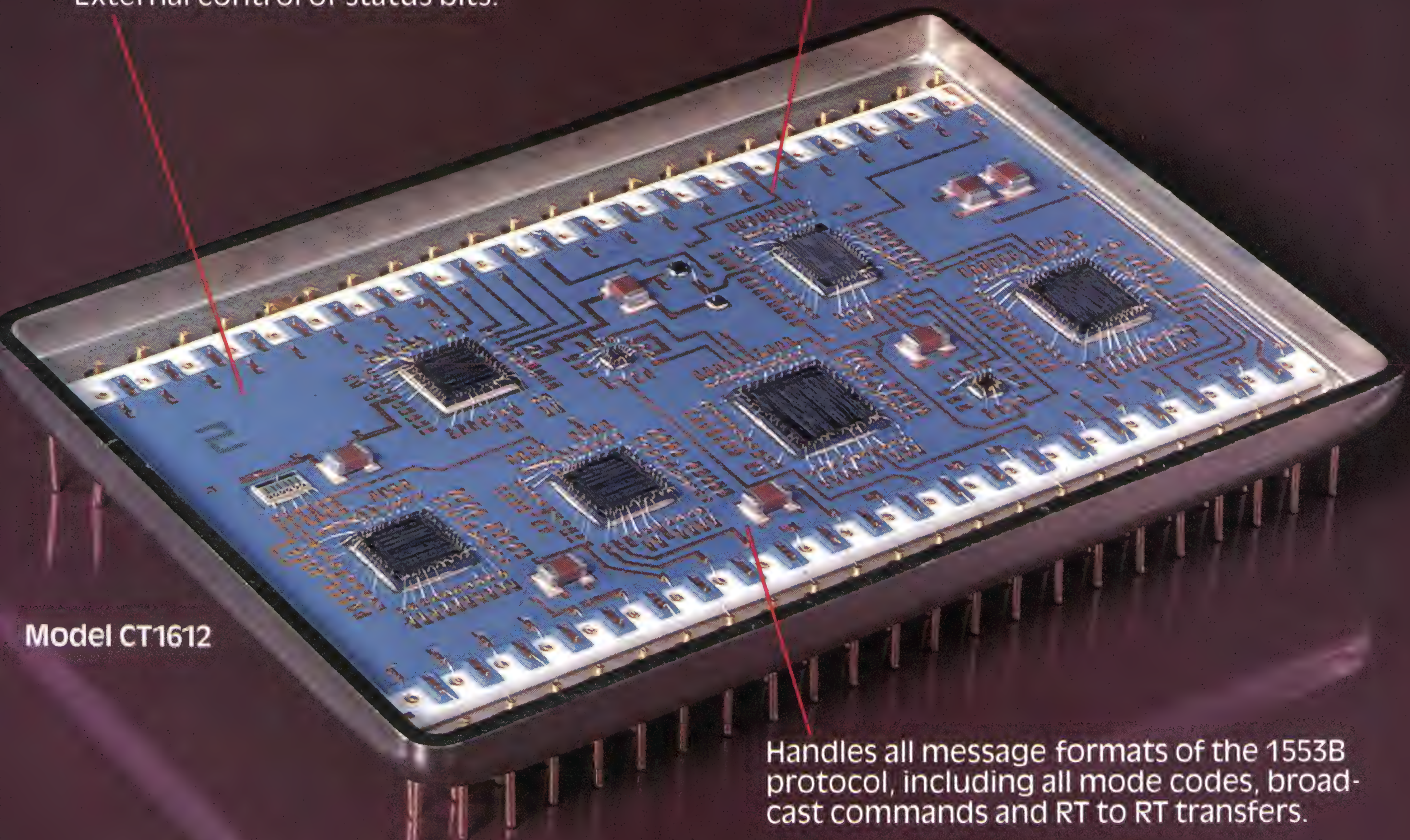


32-BIT UNIX SYSTEMS

- *Feature MC68020 μPs*
- *Support Ethernet communications and SCSI storage control*

Containing the 16.7-MHz Motorola MC68020 μP, the MCX family of 32-bit Unix-based microcomputers support Ethernet communications and SCSI storage control. The essential unit is the Model 40, which includes a 3.6-MIPS floating-point accelerator, supports as many as 12 terminals, and provides a 6-slot chassis for expansion. Intelligent communications, graphics, and data-acquisition μPs reduce the load on the system's CPU. A 12M-byte/

MIL-STD-1553B: now you can have it your way.



External control of status bits.

Converts from remote terminal to bus controller by pulling one line low.

Model CT1612

Handles all message formats of the 1553B protocol, including all mode codes, broadcast commands and RT to RT transfers.

CTI'S new programmable interface not only performs every function of the MIL-STD-1553B protocol, but it gives you other special features as well:

- Lowest power consumption available–less than 200 milliwatts!
- The terminal and subsystem flag bits are programmable.
- The message error bit can be set when illegal commands are decoded.

The CT1612 isn't just a prototype. Quantities have already been delivered for use in major programs. Find out how easy it is to have MIL-STD-1553B your way. Call or write Al DiMarino, Circuit Technology Inc., 160 Smith Street, Farmingdale, NY 11735
516/293-8686.

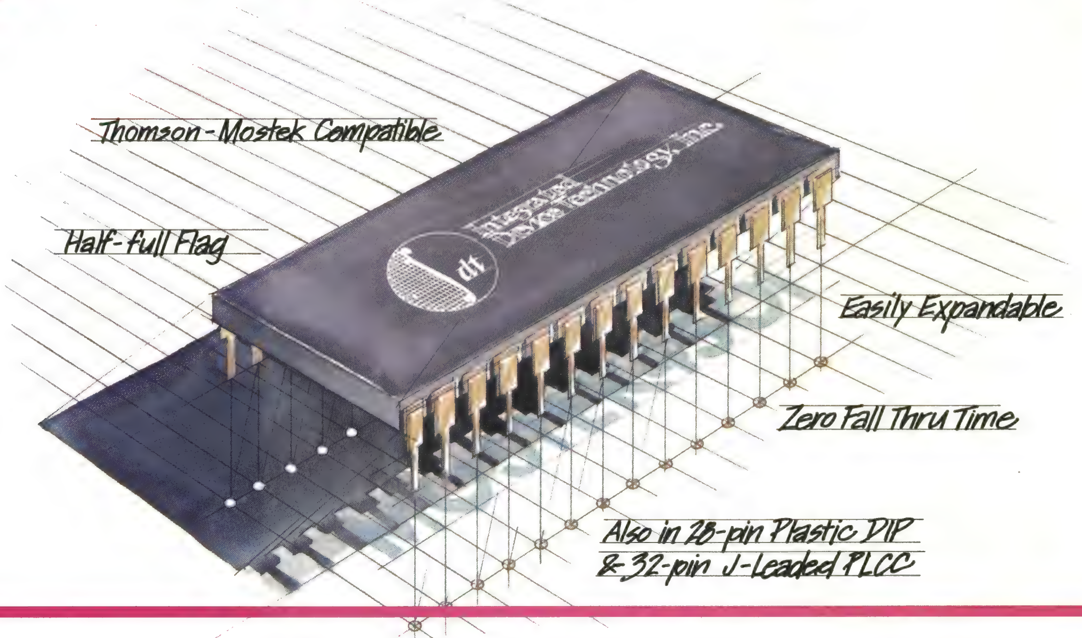
CTI
Circuit Technology Inc.
The military standard in microelectronics.

CIRCLE NO. 117

World's Biggest

1024x9 FIFO

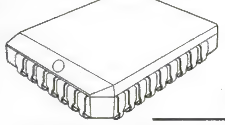
35 ~~50~~nsec ACCESS TIME


Thomson-Mostek Compatible
Half-full Flag
Integrated Device Technology, Inc.
Easily Expandable
Zero Fall Thru Time
Also in 28-pin Plastic DIP
& 32-pin J-Leaded PLCC

Some FIFOs are deep, some are fast. These FIFOs are deep. And fast.

The IDT7202 1024x9 is the deepest FIFO in the world. The IDT7201 is 512x9. Both provide the same fast 45ns read/write cycle time. Yet power dissipation is only 500mW. Our advanced CEMOS™ II technology makes it possible.

Both devices are pin and functionally compatible with the Thomson Components-Mostek MK4501 but run twice as fast. Use the IDT7201 as a pin-for-pin replacement or insert the 1024x9 IDT7202 and double the density of your existing sockets.



J-Leaded PLCC

Available now. ☐ 32-pin DIPs (both plastic and ceramic) ☐ 32-pin ceramic LCC ☐ a low-cost 32-pin J-leaded plastic PLCC and ☐ incredibly dense modules.

Features. The IDT7201/7202 are dual ported and can be written to and read from asynchronously and simultaneously. ☐ Unique RAM pointer architecture eliminates fall through time ☐ full, empty and half-full flags ('A' version) ☐ rapid data retransmit ☐ full 9-bit parity width ideal for serial communication systems ☐ easily expandable by width and depth.

Modules.

We also package four of these FIFOs, built in LCCs, on a co-fired multilayered ceramic DIP substrate. The result is two extraordinarily dense, fast, rugged low-power subsystems. *Available now.*

4Kx9 FIFO Module: IDT7M204. Com'l. access time (worst case) is 40ns.

2Kx9 FIFO Module: IDT7M203. Com'l. access time (worst case) is 40ns.

The rest of the DSP family.

Providing bipolar speed, highest quality, with CMOS power and compactness. *Available now.*

16x16 Multipliers: IDT7216/7217 replaces MPY016H/K, Am29516/17and WTL1516. Com'l. speed (worst case) is 35ns.

16x16 Multiplier/Accumulators: IDT7210 (35-bit output) replaces TDC1010. ☐ IDT7243 (19-bit output) replaces TDC1043. Com'l. speed (worst case) is 35ns.

12x12 Multipliers: IDT7212 replaces MPY012. ☐ IDT7213 is single clock. Com'l. speed (worst case) is 30ns.

12x12 Multiplier/Accumulator: IDT7209 replaces TDC1009. Com'l speed (worst case) is 30ns.

64-bit IEEE Floating Point Multiplier and ALU: IDT72064/065 replaces Weitek 1064/65—2.5 megaflops, double precision multiply. ☐ IDT72264/265 replaces Weitek 1264/65—5 megaflops, double precision multiply. *Available 4Q86.*

May we be of assistance?
Call **1-800-IDT-CMOS** or your local IDT representative for a copy of our *Application Note*—explaining how to use deep, fast FIFOs—and a *Product Selector Guide* on high-speed CEMOS™ **MICROSLICE**™ (bit-slice products), **Subsystems**, **DSP Circuits** (multipliers, MACs and FIFOs), ultra-fast **Logic** and one of the fastest, broadest lines of **Static RAMs** in the world.

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Digital Signal Processing Division

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(408) 727-6116
TWX 910-338-2070

CIRCLE NO. 118

CEMOS and MICROSLICE are trademarks of sec asynchronous memory bus facilitates 32-bit data transfers. At the high end of the family, the Model 70 can accommodate as many as four MC68020 CPUs, adds a 32-slot chassis, includes an enhanced Multibus I/O system, and gives you 4G bytes of virtual-address space per process. The MCX models come in pedestal, tabletop, and cabinet styles. $18,700 to $73,000.

Harris Corp, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309. Phone (305) 974-1700

Circle No 376

ENGINEERING PC

- *Features IEEE-488 interface*
- *Includes 80286 μP and 512k bytes of RAM*

Offering an IEEE-488 interface for engineering and scientific applications, the System 488 is an IBM PC/AT-compatible computer that supports the GPIB standard for instrument-control programming. System 488 comes with an 8-MHz 80286 μP; 512k bytes of RAM; serial and parallel ports; an IEEE-488 interface; a combined hard-/floppy-disk interface; a 1.2M-byte floppy-disk drive; an enhanced graphics display interface for color or monochrome monitors; and a monochrome monitor. The package includes DOS 3.1, Basic, Superkey, word-processing software, HP 85 graphics emulation, IEEE-488 applications, and other specialized software tools for solving engineering and scientific problems. You can optionally order 20M-, 30M-, or 40M-byte hard-disk drives and a color monitor. $3980.

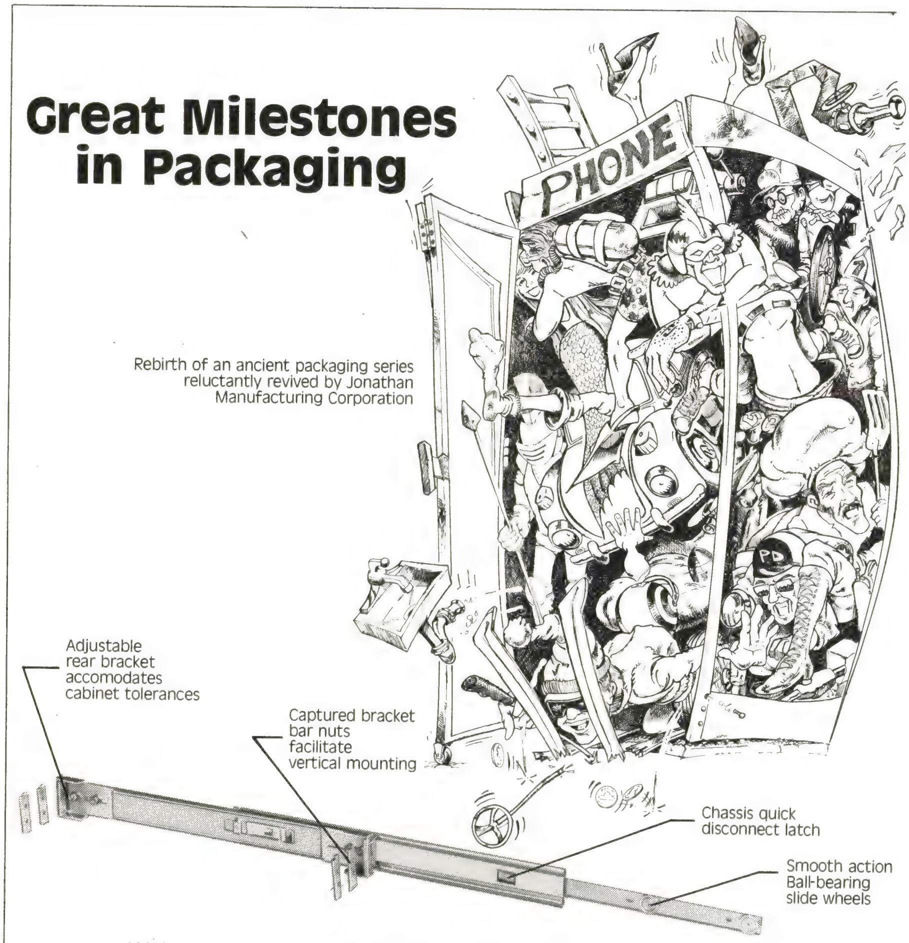
Capital Equipment Corp, 99 S Bedford St #107, Burlington, MA 01803. Phone (617) 273-1818.

Circle No 377

BAR-CODE READER

- *Scans poorly printed or damaged bar codes*
- *Beeps after successful scan*

The 9570 Wedge Reader provides bar-code recognition for IBM computers and terminals, including the PC, PC/XT, PC/AT, 3178, 3179, 3180, and 5291-2. Designed with a



Great Milestones in Packaging

PHONE
Rebirth of an ancient packaging series reluctantly revived by Jonathan Manufacturing Corporation
Adjustable rear bracket accomodates cabinet tolerances
Captured bracket bar nuts facilitate vertical mounting
Chassis quick disconnect latch
Smooth action Ball-bearing slide wheels

We're sure that Ma Bell had another idea in mind when she designed the original phone booth, but good olde Yankee ingenuity took over and was not about to let all that space go to waste–giving new meaning to the words "High Density". No easy in, easy out here. Jonathan saw this same situation arising in standard 19" cabinetry, as it lent itself more and more to high density chassis packaging but still contended with less than acceptable stick-slip access with friction chassis slides.

The answer to this predicament is Jonathan's new Series 375QD TRU-GLIDE® ball-bearing steel chassis slide. The replacement for the friction Accuride 830, Chassis Trak C-300, Grant SS-168 and Zero C-300 models, this new 75-lb. capacity slide is thin (3/8") enough to fit easily in a standard 19" cabinet, while providing smooth ball-bearing action and all the precise mounting, locking and chassis disconnect features you could want.

Don't fight with binding friction slides... when, for a few dollars more, you can put Jonathan's 30 years of packaging experience to work to smooth out all your access problems.

Jonathan Manufacturing Corp., 1101 So. Acacia Ave., Fullerton, CA 92634 • (714) 526-4651

CIRCLE NO 119

16-bit µP and a proprietary scanning algorithm, the unit allows you to scan even poorly printed or damaged bar codes. The 9570 requires no additional power when used with the manufacturer's wands and laser scanners. Two input ports on the reader let you attach multiple scanning devices. The unit also has an adjustable speaker that emits a beep after each successful scan and four LEDs that monitor the unit's operating status. $495.

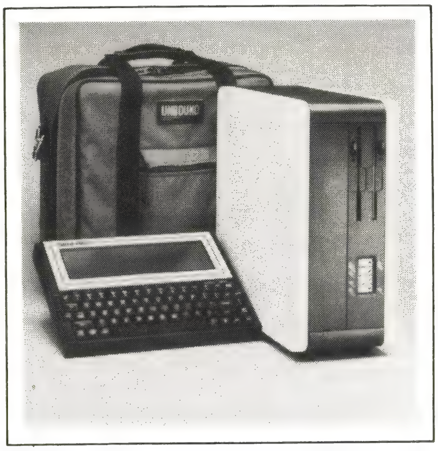
Intermec Corp, Box 360602, Lynnwood, WA 98046. Phone (206) 348-2600. TLX 3794107.

Circle No 378

PORTABLE Q BUS PC

- *Four Q Bus slots in basic model*
- *RAM expandable to 1M byte*

Incorporating a DEC-compatible Q Bus architecture, the Qube family of lightweight, modular computers gives you the freedom to carry around a personal computer with the power of a DEC system. The basic unit, called a Q1 Master Module, includes four Q Bus quad slots, 22M or 44M bytes of disk storage, and either dual floppy-disk drives or a QIC tape drive. The Q1 weighs <25 lbs and is available with a carrying bag. You can expand it by adding four additional Q-Bus slots and additional disk or tape drives. Other models give you as much as 1M byte of RAM, almost 200M bytes of disk capacity, and 16 ASCII communication lines. $6995 to $19,195.

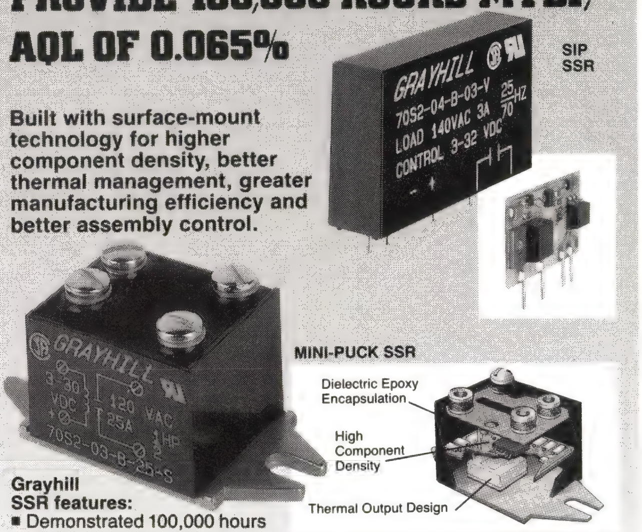


Unbound Inc, 15239 Springdale St, Huntington Beach, CA 92649. Phone (800) 862-6863; in CA, (714) 895-6205.

Circle No 379

GRAYHILL SOLID STATE RELAYS PROVIDE 100,000 HOURS MTBF, AQL OF 0.065%

Built with surface-mount technology for higher component density, better thermal management, greater manufacturing efficiency and better assembly control.


SIP SSR
GRAYHILL 70S2-04-B-03-V LOAD 140VAC 3A CONTROL 3-32 VDC 25 HZ 70
MINI-PUCK SSR
GRAYHILL 3-30 VDC 120 VAC 25A 1HP 70S2-03-B-25-S
Dielectric Epoxy Encapsulation
High Component Density
Thermal Output Design

Grayhill SSR features:
- Demonstrated 100,000 hours MTBF (test data to date)
- AQL of 0.065%
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- High blocking voltage components
- High surge current capacity
- Logic circuit compatibility
- Low EMI and RFI generation
- Inductive load switching capability
- Excellent shock and vibration immunity
- High dielectric voltage rating
- Maximum load current; minimum space
- 100% final testing
- SIP or Mini-Puck package styles
- DC-DC models available
- Competitive pricing

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CIRCLE NO 120

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Honeywell

CIRCLE NO 121

ANNOUNCING: NOW AVAILABLE FOR SHIPMENT!

The Key Tronic 101 KEYBOARD

Act now! Key Tronic has the new IBM* enhanced keyboard layout for you! With reponsiveness that's the best in the industry, Key Tronic provides a 101 keyboard which:

- **Features IBM* enhanced layout.**
- **Includes Key Tronic reliable switch technology and quality.**
- **Is ready for shipment now!**

If you want the IBM* enhanced layout, the Key Tronic 101 keyboard is for you. If the 101 is not for you, we have alternative layouts available for immediate shipment. Of course, customized versions are also available.

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The Key Tronic 101 layout features include:

- Separate cursor & numeric pad
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- 12 function keys
- Break over tactile feel
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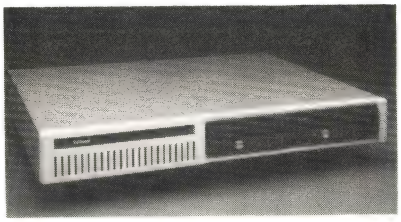
CIRCLE NO 157



HARD-DISK SUBSYSTEM

- *Offers combination of removable and fixed disk drives*
- *Has 7.5-bps data-transfer rate*

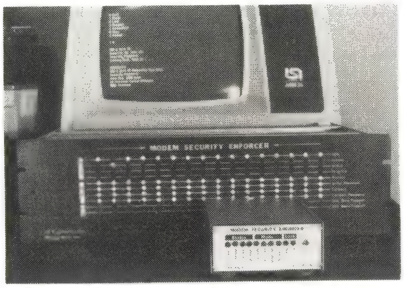
The SQ1500 hard-disk subsystem gives you unlimited storage capacity for your IBM PC, PC/XT, PC/AT, or compatible computer. The subsystem is available in four models: a single 15M-byte removable drive, two 15M-byte removable drives, a 15M-byte removable drive and a 45M-byte fixed drive, and two 45M-byte fixed drives. The subsystem's chassis measures 15×19×2.5 in. and fits between your PC's monitor and CPU. The subsystem provides a data-transfer rate of 7.5M bps. You can order a development package that includes a chassis, a controller, utility software, two removable disk cartridges, cables, mounting brackets, and an instruction manual. $2499 to $3695.

SyQuest Technology, 47923 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 490-7511. TWX 910-381-7027.

Circle No 380

MODEM SECURITY

- *Connects via RS-232C ports*
- *Offers callback feature*

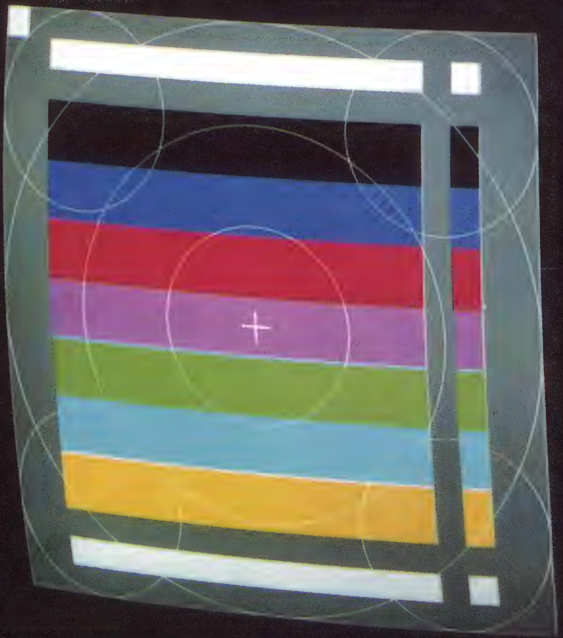


You can protect your dial-up modem from unauthorized access with the MSE-1 modem security enforcer. The device connects between your modem's RS-232C plug and your computer's RS-232C port. It prompts callers for a user name and optional password. After recognition, the MSE-1 terminates the call and dials a stored telephone number that is associated with the user name. (If you wish, you can use the unit without its callback feature.) Each modem handles one telephone line. For multiple phone lines, you can order the CAGE-MSE, which can house as many as 16 MSE-1 units. You can further expand the system to include multiple cages. From $300.

IC Engineering Inc, Box 321, Owings Mills, MD 21117. Phone (301) 363-8748.

Circle No 381

You Don't Need a Thousand Words When You Have a Picture Like This!



Unretouched photograph

*3.5 NS max. rise & fall time measured at CRT cathode

The image quality demonstrated here is required by your customers . . . and will be appreciated! They expect THE BEST from original equipment manufacturers. You can provide it! While other video monitor venders claim, "about 100 + MHZ" video bandwidth,* **Video Monitors, Inc.** provides it! While other vendors claim, "full gray-scale color capability," **VMI** delivers it!

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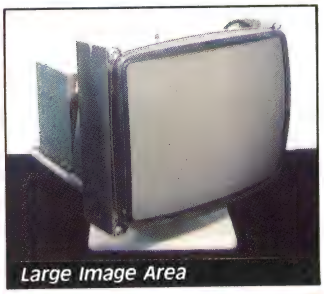
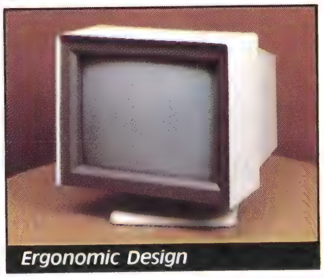
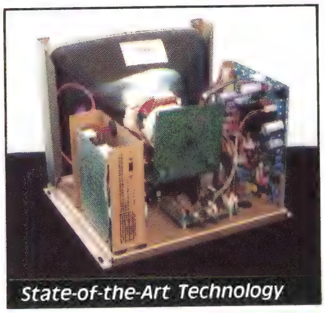


Large Image Area

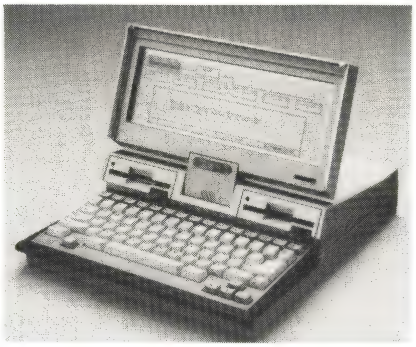


Ergonomic Design



State-of-the-Art Technology

CIRCLE NO 124



LAP-TOP PC

- *Dual 720k-byte 3½-in. floppy disks*
- *256k bytes of RAM*

Weighing <13 lbs, the PC Convertible features dual 720k-byte 3½-in. floppy-disk drives and a detachable LCD. You can purchase an optional 9-in. composite video display with 640×200 graphics resolution or a 13-in. RGB direct-drive display with 320×200-pixel resolution. The unit comes with 256k bytes of RAM and has a built-in, sloped, 78-key keyboard. You can expand the unit's RAM to 512k bytes. Options include a serial/parallel adapter, an internal modem, a CRT display adapter, and a dot-matrix printer that attaches to the back of the computer. The computer is battery-powered, and depending on disk-drive and printer usage, it can run from six to 10 hours before the battery pack requires recharging. $1995.

IBM Corp, Entry Systems Div, Box 1328, Boca Raton, FL 33432. Phone (305) 982-3474.

Circle No 427

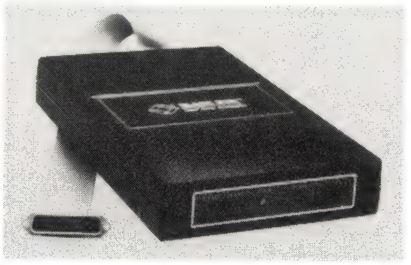
OPTICAL STORAGE

- *Plugs into VAX computer*
- *Requires no hardware or software changes*

This optical storage peripheral, the OAS 4300, requires no changes to host hardware or software. The unit operates in three application modes: on-line, off-line, and pass-through. In its on-line mode, the OAS 4300 appears to the host as a tape formatter and drive and uses standard I/O commands. In its off-line mode, the OAS 4300 lets you control tape-to-disk and disk-to-tape data transfers without host intervention, using menu-driven software accessed through the OAS terminal. You can copy an entire tape, records between file marks, or a specific number of records. The menu also lets you display the optical disk's directory and compare data from disk and tape for copy verification. The pass-through mode lets your host communicate through the peripheral. From $38,500.

Aquidneck Data Corp, 170 Enterprise Center, Middletown, RI 02840. Phone (401) 847-7260.

Circle No 428



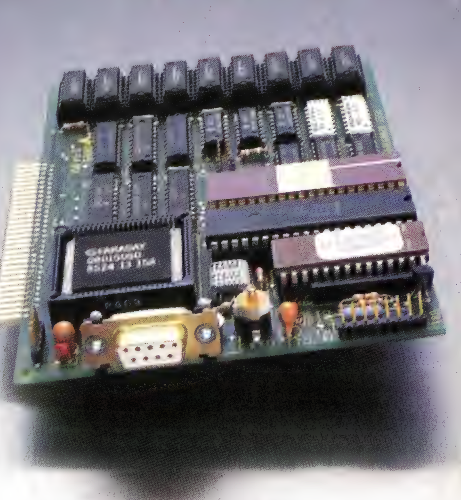
ERROR CONTROLLER

- *Offers selectable baud rates*
- *Permits communication among dissimilar machines*

The MNP error controller lets you transmit error-free data at 300 bps, 1200 bps, or 2400 bps. The MNP uses a networking protocol that permits data communications among similar and dissimilar PCs, networks, or mainframes. When the device detects a transmission error, it automatically sends the data block back until the data is transmitted and received accurately. You can also limit the number of times a data block is retransmitted. The unit can automatically determine whether its error-checking protocol is in use at the receiving terminal. $295.

Black Box Corp, Box 12800, Pittsburgh, PA 15241. Phone (412) 746-5500.

Circle No 429



smallest

Faraday delivers the Micro PC.™ A single board computer with the capabilities of the IBM® PC but only 4.2x6.2 inches.

With the Faraday Micro PC, you can imbed the power of the IBM PC into thousands of new applications. The Micro PC features: ■ Plug-in card ■ ROM BIOS on board ■ 8088 processor with optional 8087 co-processor ■ 256K RAM memory ■ 64K ROM memory ■ CMOS version optional ■ 4.77 mhz

You can depend on Faraday to deliver 100% PC BUS compatibility. We supply OEMs in telecommunications, office automation, industrial automation, instrumentation, manufacturing test equipment, medical instruments, point of sale, computer terminals and personal computing applications.

For more information on the Micro PC or other Faraday PC BUS single board computers, call us at 408-749-1900.

Faraday Electronics, 749 North Mary Avenue, Sunnyvale, California 94086, TLX 706738. In England, TLX 847096 EMDAL.

FARADAY

Faraday quality at ⅕ the size.

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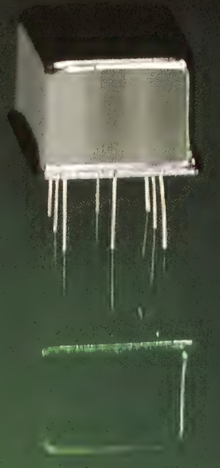
CIRCLE NO 183

SPACE INVADER.

SPACE SAVER.

TO-5 (FORMED)



HI-G MINIGRID™

The next generation TO-5 relay is square.

It's time for the round relay to move over. The square MiniGrid relay is here . . . with all the performance and reliability you've come to expect from the TO-5 relay.

MiniGrid relays, from Hi-G, present no pinout or spacing problems. 0.100 pin spacing permits direct insertion into PCB's without costly forming operations needed for the standard TO-5 . . . especially where space is at a premium.

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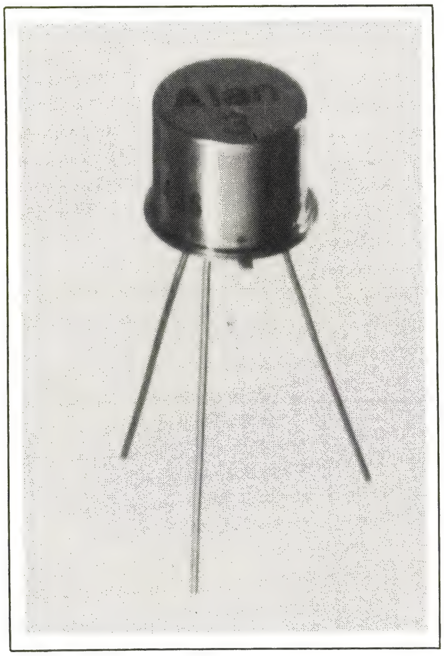
CIRCLE NO 126

NEW PRODUCTS

COMPONENTS & PACKAGING



ATTENUATORS

- *Available in 1- to 20-dB values*
- *DC to 500-MHz range*

Designed for socket or pc-board mounting, the PI Series attenuators are packaged in a 0.25×0.36-in. case with three 0.5-in. leads. They are available in attenuation values from 1 to 20 dB and feature a dc to 500-MHz operating range. Accuracy is 0.5 dB; impedance is 50Ω nominal. $20.

Alan Industries Inc, Box 1203, Columbus, IN 47202. Phone (800) 423-5190.

Circle No 382

PRESSURE SENSORS

- *Static accuracies of ±0.1%*
- *TO-8 and TO-5 packages*

The Nova-P Series TO-8 and TO-5 packaged silicon pressure sensors exhibit static accuracies of ±0.1% (combined linearity, hysteresis, and repeatability effects) and operate over the 0 to 70°C range. Output-signal level is 100 mV at 1.5-mA input. Devices are available in full-scale pressure ranges of 0 to 30 kPa and 0 to 100 kPa in either gauge or absolute versions. The packages are equipped with a $\frac{3}{16}$-in. outer-diameter-pressure input port. The manufacturer has designed the sensors to operate in moist air. $12. Delivery, stock to eight weeks ARO.

NovaSensor, 2975 Bowers Ave, Santa Clara, CA 95050. Phone (408) 988-4540.

Circle No 383

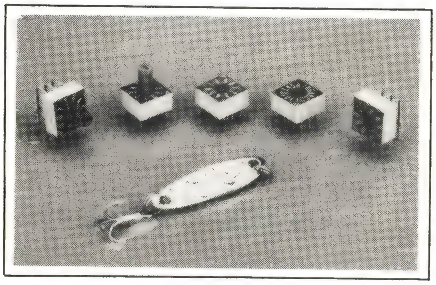
SMT KITS

- *Offers 575 SMT components as an option*
- *Features prototyping boards, component attachments*

Two configurations of the SMT (surface-mount technology) Training Kit are available. The SMT2000, in addition to hardware, contains over 575 surface-mount components, including chip resistors, chip capacitors, diodes, and transistors. The SMT1000 is intended for those who already have a supply of component parts. Both configurations have prototyping boards, component attachment and interconnection materials, and a 50-pg manual. Devices furnished with the SMT2000 include 270 surface-mount multilayer ceramic-chip capacitors of assorted values from 100 pF to 0.033 μF; 300 resistors ($\frac{1}{8}$W in assorted values from 22Ω to 150 kΩ); 10 diodes in SOT-23 packages; and 10 transistors in SOT-23 packages. Both configurations include five different double-sided, epoxy-glass circuit boards with tinned footprint patterns for SOIC and PLCC ICs; plated-through holes; and ground buses according to SMT device standards. Layout paper and planning sheets are furnished as well. Both versions have a sixth board configured with different PLCC patterns. SMT2000, $348; SMT1000, $215.50.

Vector Electronic Co, 12460 Gladstone Ave, Sylmar, CA 91342. Phone (818) 365-9661.

Circle No 384



DIP SWITCH

- *Allows you to rotate shaft to select code*
- *Features O-ring with sealed terminals*

The 3300 Series Micro-DIP switch allows code selection by rotating a shaft to the desired position. The board requires less space because of the switch's size and internal seal, and process-seal removal is not necessary once the pc board has gone through the flow-solder and wash cycles. An integral O-ring and epoxy-sealed terminals, which protect the switch from contamination during and after solder and cleaning, provide permanent sealing. The switch is available in top- and side-adjustable models with either a flush or extended actuator shaft. The 10- or 16-position (hexadecimal) switches have single-pole binary-coded-decimal or complementary codes that make the switches suitable for digital logic applications. 330002GS, $3.05.

EECO Inc, Box 659, Santa Clara, CA 92702. Phone (714) 835-6000. TWX 910-595-1550.

Circle No 385

DRIVER/RECEIVER

- *Comes in 20-pin SIP*
- *Operates over 0 to 19k bps*

The CH1165A hybrid quad line driver/receiver provides the standard interface between data-terminal equipment and data-communications equipment as defined by EIA standard RS-232C. The 20-pin device's filters comply with FCC, Part 15. The driver operates over a data-rate range of 0 to 19.2k bps; its input is compatible with standard TTL circuits. The circuit uses 5 and ±12V. The unit measures 0.135×0.5×2 in. $9.92 (500).

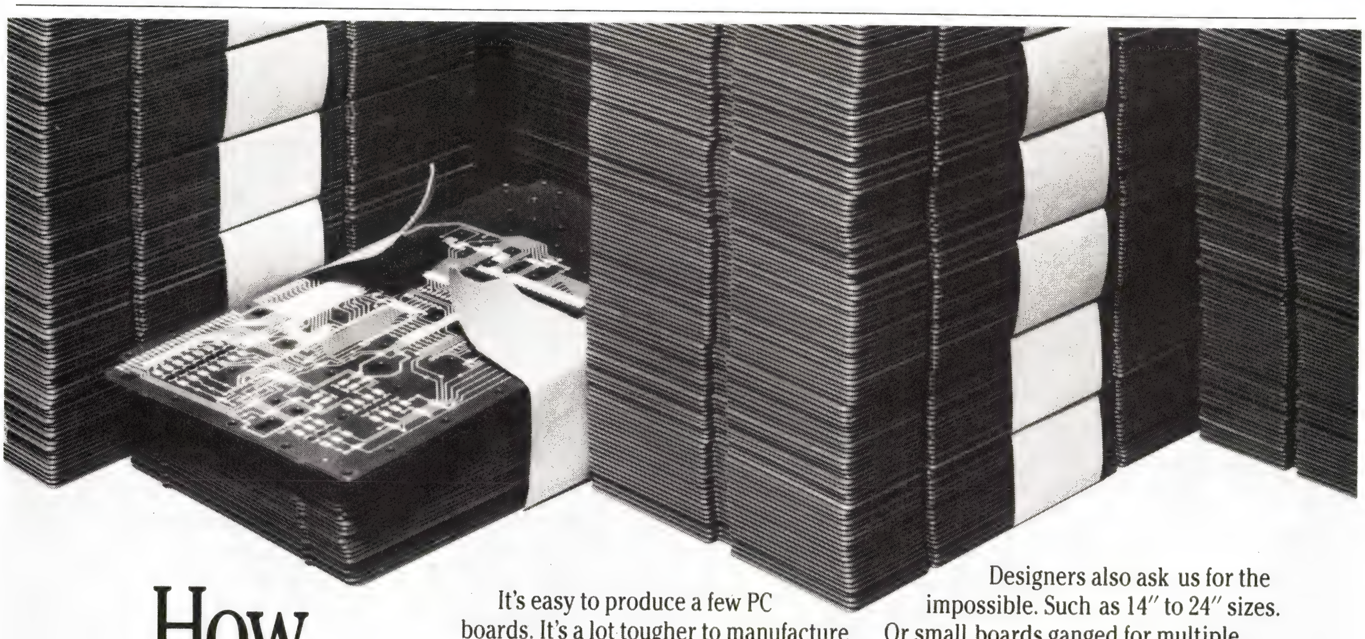
Cermetek Microelectronics Inc, Box 3565, Sunnyvale, CA 94088. Phone (408) 734-8150. TWX 910-379-6931.

Circle No 386

STEPPER TRANSLATOR

- *Speeds of 15,000 steps/sec*
- *5A max phase current*

The THD-1801D compact translator features 5A max phase current and a maximum step rate of 15,000 steps/sec. It operates at output voltages from 22 to 40V dc and comes on a single board. The unit accepts pulses from external devices such as



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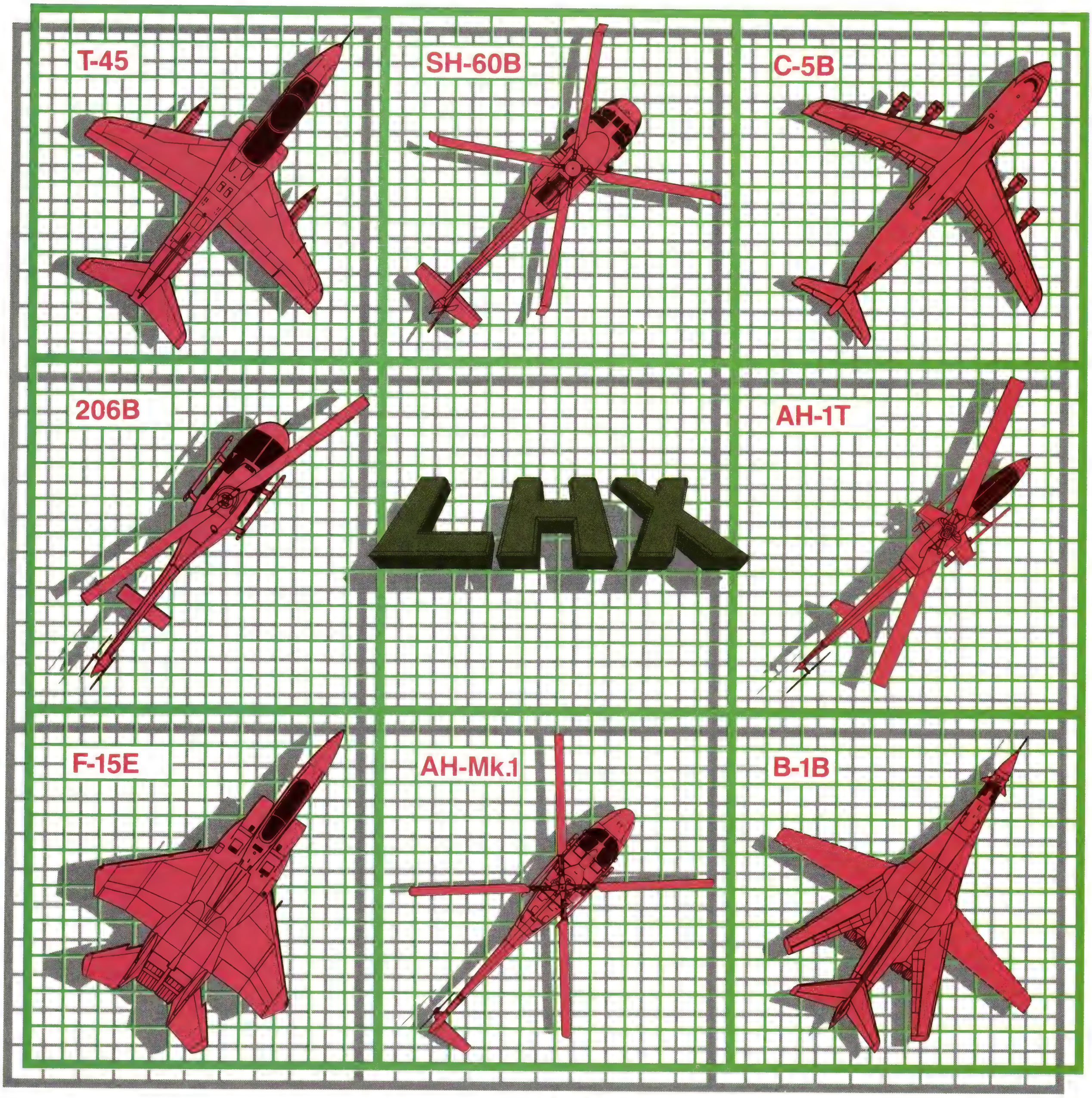

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Or work with the team that designed the first new air variable capacitor technology in 20 years, including the only capacitor to use the substrate as the capacitor stator, for a precision tuning device ideal for ceramic and miniature circuits.

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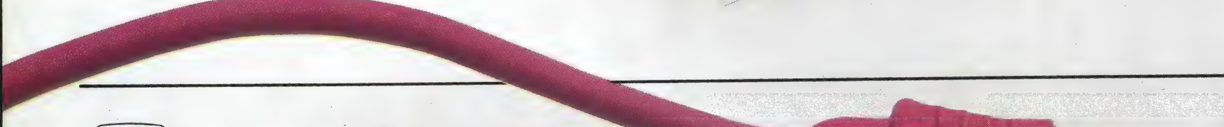

The Stripline process, terminating 2,000 and more pieces per hour, is ideal for insert molded products, such as this test instrument patch cord.

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E. F. JOHNSON COMPANY, WASECA, MINN. 56093
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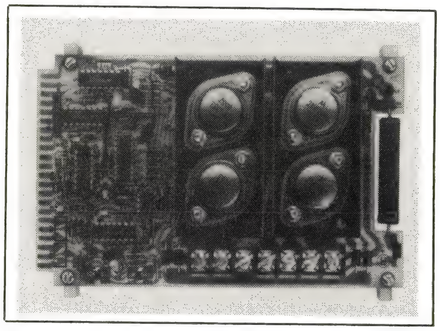
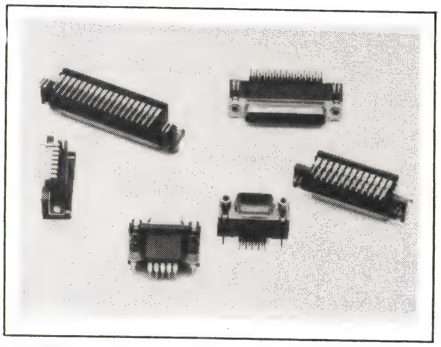


a computer or a programmable logic controller; each pulse produces a single 1.8 to 0.9° motor step. The exponential acceleration and linear deceleration curves allow reductions in traverse times. Acceleration and deceleration times are separately adjustable from 50 to 500 msec via onboard potentiometers. The device's inputs connect to a computer's parallel port or a programmable logic controller's outputs. You can activate the device manually by switch as well. I/O connections are via a 22-pin edge connector; inputs are TTL compatible, but 12V CMOS compatibility is available as an option. A barrier-block terminal strip provides low-resistance output connections to stepper motors, series and suppression resistors, power supply, and fuses. $120.

Bodine Electric Co, 2500 W Bradley Pl, Chicago, IL 60618. Phone (312) 478-3515.

Circle No 387



CONNECTORS

- *Come with grounding brackets*
- *Offer continuous grounding*

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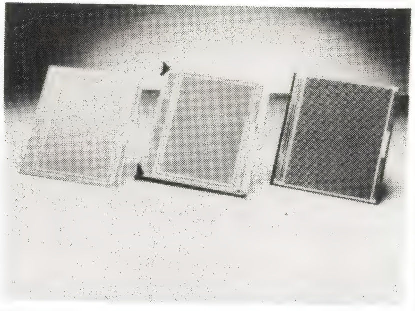
CIRCLE NO 133

into a pc board. The connectors furnish a continuous grounding path from the shell to the pc board. Five configurations are available that differ in grounding techniques: Style DG uses a solder tail to align the first row of contacts; the LG style aligns the first row as well but does so with a lock-pin approach. The SG style uses the lock pin but goes through the mounting hole, and the TG style is a top ground that uses mounting screws to ground the connector to the board. Finally, the BG style runs a strap under the D-subminiature and terminates at the mounting hole; the strap is recessed. Mounting styles include through hole, flush threaded insert, hex standoff, and round standoff. The company offers 9-, 15-, 25-, and 37-position receptacles. The connectors are UL listed and CSA certified with UL 94V-0 materials. A 25-position connector, $2.30 (5000).

Viking Connectors Co, Box 2379, Chatsworth, CA 91311. Phone (818) 341-4330.

Circle No 388



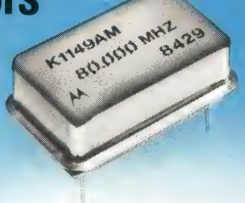
PROTOTYPING BOARDS

- *For VME and Multibus II*
- *Designed with 0.1-in. universal grid pattern*

These Eurocard prototyping boards have a 0.1-in. universal grid pattern and can accommodate any IC on a 0.1^2 in. grid in either vertical or horizontal orientation, which allows nonrestrictive placement of components. Twelve models are available in sizes from 160 mm×3U to 400 mm×9U. The boards' bus-connector

ECL Compatible Crystal Clock Oscillators

K1149
Series



- 40–125 MHz
- Complementary Outputs Available
- Various Pinouts Available

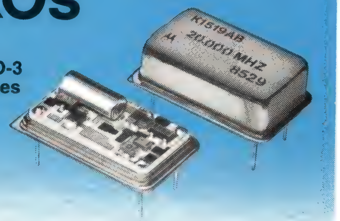
The ECL K1149 series crystal clock oscillators are compatible with the MECL 10K and 10KH logic families. The 10KH based design of the K1149 series oscillators provides improved rise and fall times, duty cycle, noise margins and power supply rejection over that of the earlier 10K family while retaining compatibility. The frequency range is from 40 to 125 MHz, with a stability of ± 100 ppm. The oscillators have an open emitter ouput which allows the user to select the load termination to optimize performance.

The all-metal hermetically sealed package, which can be wave soldered or plugged into a standard DIP socket, requires only 0.820″ by 0.520″ board space and a seated height of 0.270″.

CIRCLE 134 ON READER SERVICE CARD

DIP-Size TCXOs

MDO-3
Series



- Inclusive ± 5 ppm Stability
- DIP-Compatible Pinout

The MDO-3 Series TCXOs are enclosed in all-metal, welded packages for full hermetic seal. They feature ± 5 ppm stability, inclusive of variations in voltage, load, and humidity over a −30°C to +70°C temperature range. They cover a frequency range of 10 MHz to 26 MHz and operate from a +5V dc source.

The MDO-3 series oscillators provide a sine-wave output, and are capable of driving digital ECL or CMOS logic using circuitry described in Application Note #151, available upon request.

CIRCLE 212 ON READER SERVICE CARD

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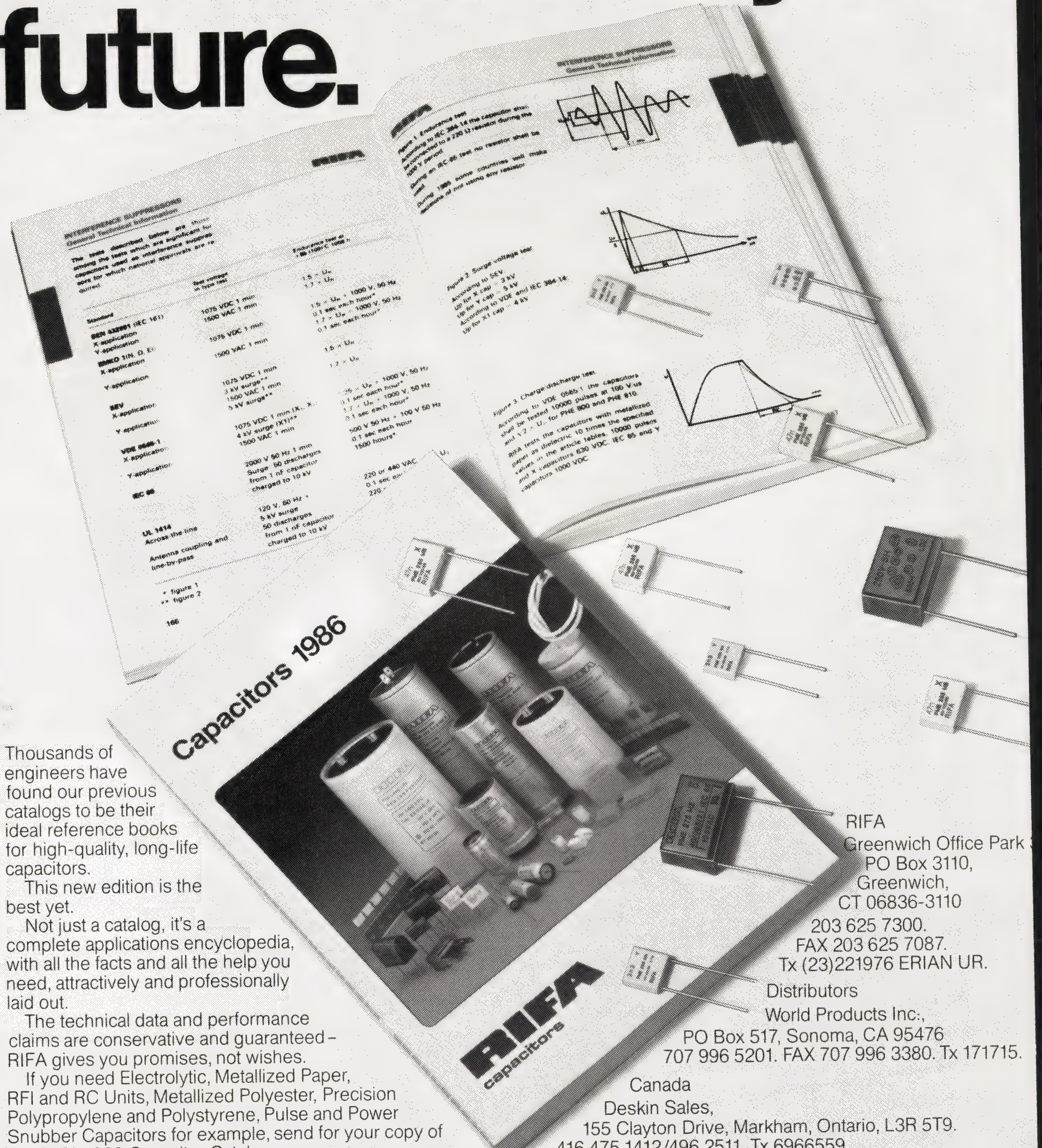

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area accepts right-angle, 96-pin wire-wrap connectors that allow direct connection to power and ground buses; the I/O area provides for mounting D-subminiature and 0.2×0.1-in. flat-ribbon cable connectors. Three signal-area patterns are available: pad per hole; buses only, with power and ground buses following the perimeter of the card; and power and ground plane, with one side of the board covered with ground plane and the other covered with a power plane. The boards use eyelets to commit power and ground to connectors by soldering. You can use the same eyelets to connect the power and ground foils anywhere on the board surface. Individual drilled holes in the power and ground foils have isolated rings around them to prevent inserted leads from shorting. $15 to $39.

Vector Electronic Co, 12460 Gladstone Ave, Sylmar, CA 91342. Phone (818) 365-9661.

Circle No 389

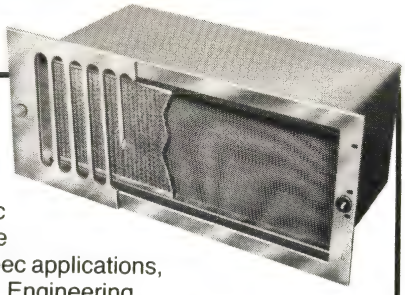
CONNECTORS

- *Gold-plated contact areas*
- *Flat-cable and solder-dip types available*

The AXC card-edge connectors feature gold plating over the contact area and antiporosity treatment. Both solder-dip and flat-cable types (with or without flanges) are available and permit various methods of chassis mounting. Electrical rating is 3A for solder-dip type and 1A for flat-cable type. The solder-dip connectors are available with 34 to 86 contacts; the flat-cable type is available with 20 to 60 contacts. Housings are glass-reinforced PBT with a UL rating of 94V-0. $1.75. Delivery, stock to six weeks ARO.

Aromat Corp, 250 Sheffield St, Mountainside, NJ 07092. Phone (201) 232-4260. TWX 710-997-9536.

Circle No 390



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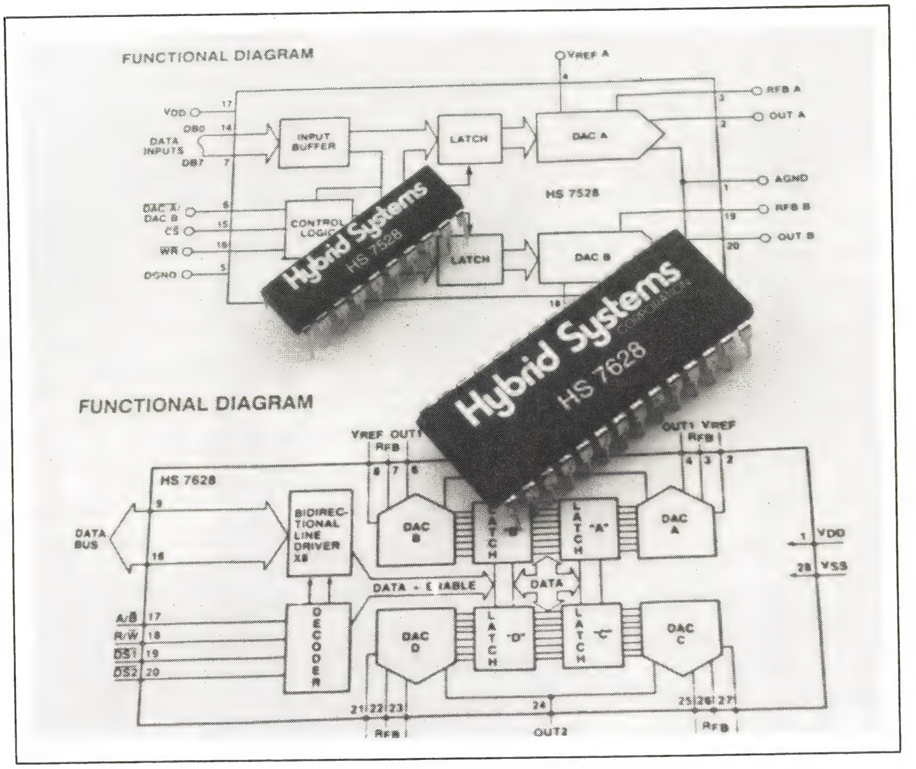


D/A CONVERTERS

- *Several converters on a single monolithic chip*
- *Choice of dual or quad D/A converters*

The HS7528 dual 8-bit D/A converter and the HS7628 quad 8-bit D/A converter incorporate multiple D/A converters on a single monolithic chip. The dual D/A converter, contained in a 0.3-in.-wide, 20-pin DIP, offers 4-quadrant multiplication with a separate reference input and feedback resistor for each chip. Differential linearity specs at ±½ LSB max and relative accuracy (integral linearity) at ±¼ LSB. Current-output settling time is 80 nsec, and gain error is ±1 LSB. The dual D/A converter operates from a 5 to 15V power supply and dissipates 20 mW. It's bus compatible with most 8-bit μPs, including the 6800, 8080, 8085, and Z80. The HS7628, housed in a 28-pin DIP, contains an input register that transfers data to any of the four D/A-converter latches. The device operates from a 5V supply and dissipates 20 mW max. Integral and differential nonlinearity are ±½ to ±⅛ LSB, depending on grade. Gain error ranges from ±1.8% to ±0.5% FSR (full-scale resolution) and gain-error TC is 2 ppm/°C max. Settling time is 750 nsec max. HS7528, $5.80 to $29.30; HS7628, $8.92 to $44.80 (100).

Hybrid Systems Corp, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 391

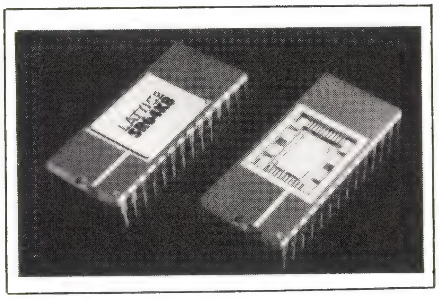
CMOS PLD

- *Mask-programmable version of bipolar PAL device*
- *32 macrocells implement more than 1500 equivalent gates*

The Model ZHAL64R32 CMOS PLD is a mask-programmable version of the bipolar MegaPAL device (PAL64R32). The maximum supply current at 16 MHz is 300 mA, compared with the 640 mA drawn by the bipolar part. The device features 32 macrocells for implementing more than 1500 equivalent gates. It has 64 device inputs and 32 registered outputs. Other features include four independent clocks; HC- and HCT-compatible inputs and outputs; product-term sharing and register bypass; and selectable polarity, which enables the outputs to be either active high or active low. The device operates from 4.5 to 5.5V supplies. Maximum operating frequencies are 16 MHz (commercial) and 14 MHz (industrial). In an 84-pin plastic LCC, $24 (1000).

Monolithic Memories Inc, 2175 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 970-9700. TWX 910-338-2376

Circle No 392



STATIC RAM

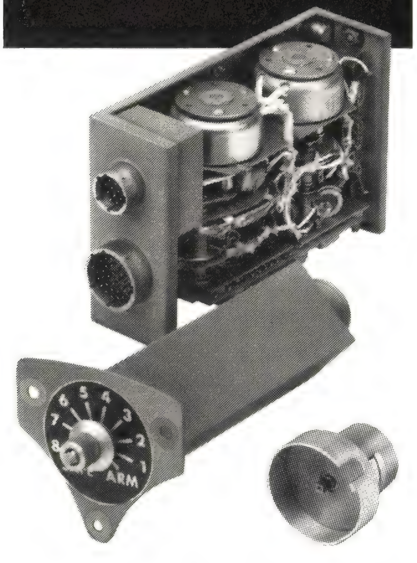
- *Provides four times the capacity of 2k×8-bit static RAM*
- *Can achieve 35-nsec access time*

The SR64K8 static RAM is an upgrade of industry-standard 2k×8-bit static RAMs; it provides four times the capacity while consuming approximately the same power. The RAM is also available with 35-, 45-, or 55-nsec access times. In a 28-pin, 300- or 600-mil ceramic package and a 35-nsec access time, $59.85 (100).

Lattice Semiconductor Corp, Box 2500, Portland, OR 97208. Phone (503) 629-2131. TLX 277338.

Circle No 393

Mil-spec design & retrofit advantages



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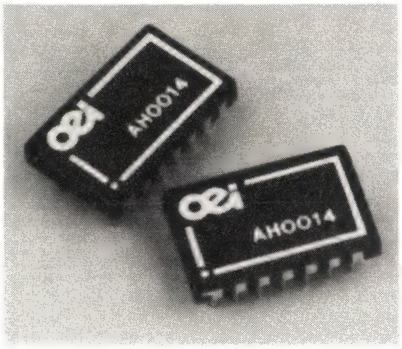


OP AMP

- *1000-MHz gain-bandwidth product at a gain of 40 dB*
- *FET front end offers high-input impedance*

The Model AH0014 wideband, low-noise operational amplifier features a typical gain-bandwidth product of 1000 MHz at a gain of 40 dB. The FET front end presents a high-input impedance of approximately 100 GΩ, an open-loop gain of 100 dB at 10 kHz, and a high CMRR without sacrificing noise performance and bandwidth. The device can supply ±10V and 10-mA drive current into a 1-kΩ load. The amplifier's operating temperature is 0 to 70°C. In a 14-pin ceramic DIP, $58 (100).

Optical Electronics Inc, Box 11140, Tucson, AZ 85734. Phone (602) 624-8358. TLX 283347.

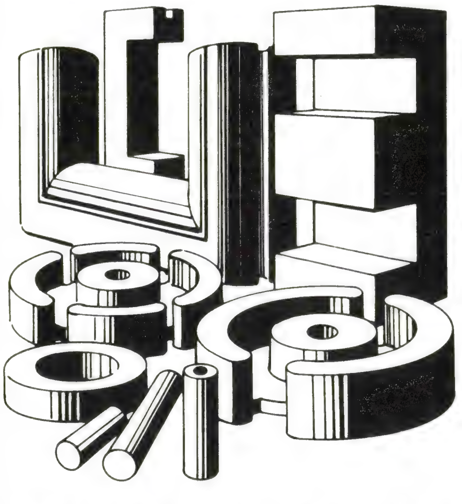
Circle No 394

GRAPHICS ICs

- *Support chips for advanced CRT controller*
- *System resolution is 640×480 pixels*

The HD63485 graphics memory-interface controller (GMIC) and the HD63486 graphics video-attribute controller (GVAC) are support chips for the manufacturer's HD63484 advanced CRT controller (ACRTC). The GMIC controls memory access for graphics display and drawing. It has built-in bus drivers that can deliver 24 mA, and circuitry to interface directly to the system's frame-buffer dynamic RAM without

LINEAR FERRITES



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Feature Size:2μ CMOS

	N-Channel	P-Channel
VTEO	$0.5–1.0_V$	$0.5–1.0_V$
BVDSS	$>10_V$	$>10_V$
$K^1 = \frac{\mu c}{2}$ linear region	21–25	6.5—8.5
B_E(Long Channel)	$0.8–1.2_V{}^{1/2}$	$0.4—0.6_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	8–10	8–10
Cap. Poly to Sub 10^4 PF/cm^2	0.55–0.65	0.55–0.65
Cap. Metal to Sub 10^4 PF/cm^2	0.27–0.32	0.27–0.32
Junction Depth	0.4μ–0.6μ	0.2μ–0.4μ
P-Well Junction	2.5μ–3.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	20–40Ω/□	60–100Ω/□
VTF Poly	$>10_V$	$>10_V$
ΔW	—1.0μ	—1.2μ
LEFF	1.0μ–1.4μ	1.3μ–1.7μ
Substrate Resistivity	2.5KΩ/□	1.2Ω/cm

Feature Size:3μ CMOS

	N-Channel	P-Channel
VTEO	$0.5–1.0_V$	$0.5–1.0_V$
BVDSS	$>10_V$	$>10_V$
$K^1 = \frac{\mu c}{2}$ linear region	18–21	6–8
B_E(Long Channel)	$0.8–1.4_V{}^{1/2}$	$0.4—0.6_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	5.9–7.0	5.9– 7.0
Cap. Poly to Sub 10^4 PF/cm^2	0.45–0.55	0.45–0.55
Cap. Metal to Sub 10^4 PF/cm^2	0.2–0.25	0.2–0.25
Junction Depth	0.6μ–1.0μ	0.4μ–0.8μ
P-Well Junction	3.5μ–4.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	10–30Ω/□	30–70Ω/□
VTF Poly	$>10_V$	$>10_V$
ΔW	—1.0μ	—1.0μ
LEFF	1.4μ–2.0μ	1.8μ–2.4μ
Substrate Resistivity	2.5KΩ/□	1.0–1.5Ω/cm

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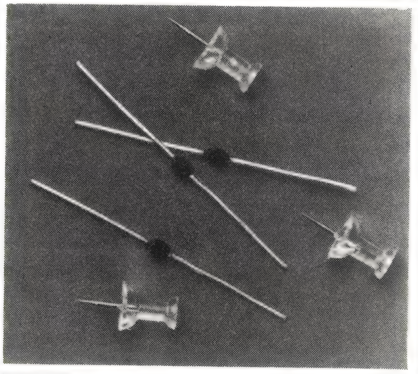
requiring external circuits. The device also generates clocking and load signals that the GVAC uses when performing horizontal zoom and scrolling functions. The GVAC provides internal shift registers and control circuits to convert data from the frame buffer to serial video signals that are used to drive the CRT at dot rates as high as 64 MHz. The bit length of the shift register is user programmable for color graphics and gray-level graphics applications. One GVAC supports 16 colors; multiple GVACs provide as many as 64k colors. A typical system consisting of the ACRTC, GMIC/GVACs, frame memory, and D/A converters can provide 640×480-pixel graphics resolution with a high-speed drawing rate of 500 nsec/pixel. Both the GMIC and the GVAC operate from a single 5V supply and provide TTL-compatible I/O levels. Housed in 64-pin plastic DIPs, both ICs cost $18 (OEM qty).

Hitachi America Ltd, Semiconductor and IC Div, 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 942-1500. TWX 910-338-2103.

Circle No 395



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vices have 0.060-in.-diameter leads for enhanced heat-sinking purposes. The SHM devices have 0.030-in.-diameter, 1-in.-long leads. Both series are available in three families: standard recovery (5 µsec), fast recovery (150 nsec), and ultrafast recovery (60 nsec). Housed in small, leaded glass packages, the rectifiers cost $2 to $30.

Solid State Devices Inc, Box 577 La Mirada, CA 90637. Phone (213) 921-9660. TWX 910-583-4807.

Circle No 396

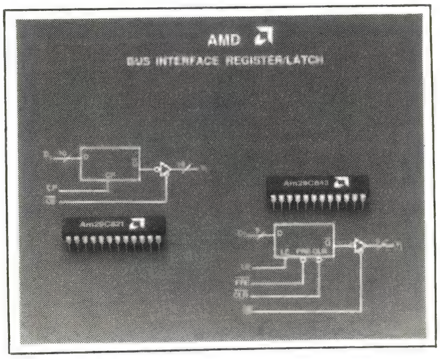
INTERFACE ICs

- *Reduce power consumption*
- *Flow-through pinout*

The Am29C821 and -843 are CMOS versions of the manufacturer's industry-standard Am29800 bipolar interface family. According to the manufacturer, the -821 10-bit-wide bus-interface register and the -843 9-bit-wide bus-interface latch reduce power consumption by more than 80% over bipolar versions of these devices. Their wide data paths allow efficient design of 16-, 32-, and 64-bit systems. The interface ICs feature a flow-through pinout; ie, all inputs are on one side of the device and all outputs are on the other side. In 24-pin plastic DIPs, $2.20 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 397



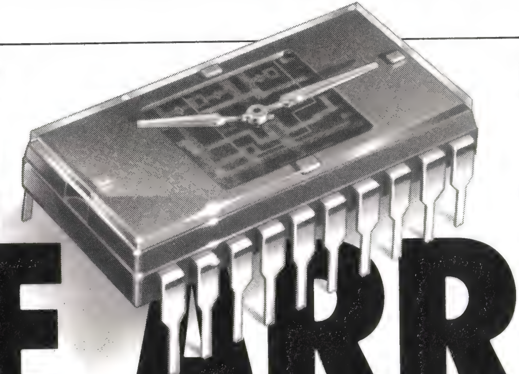
D/A CONVERTERS

- *Devices furnish 16-bit accuracy*
- *Linearity error spans 0.0015% to 0.003%*

The LH and CH versions of the DAC700 to -703 family of 16-bit D/A converters have integral linearity error of ±0.0015% of FSR max at 25°C and ±0.003% of FSR max at rated operating temperature. Total full-scale gain drift is limited to ±10 ppm/°C max for bipolar models. Digital inputs are binary coded and are TTL, LSTTL, 54/74C, and 54/74HC compatible over the operating-temperature range. Several versions cover ranges spanning −60 to +150°C. Available outputs are 0 to 10V, ±10V, 0 to −2 mA, and ±1 mA. In hermetic 24-pin ceramic side-brazed packages, $44 (100).

Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 398



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NEW PRODUCTS

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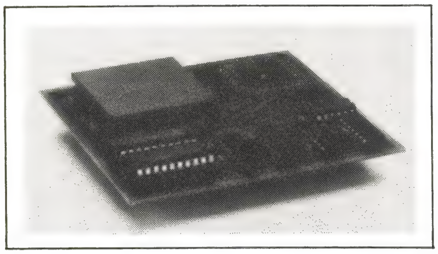


TRANSLATOR

- *Transforms PC/AT into 80386 programming environment*
- *Runs 80386 PL/M compilers and assemblers under MS-DOS*

The 386 Translator plugs into the 80286 CPU pin-grid-array (PGA) socket of an IBM PC/AT or compatible computer (including this company's PC/AT-compatible computer) and transforms the system into an 80386 programming environment, according to the manufacturer. It allows your 80286 machine to run 80386 PL/M compilers and assemblers that operate under standard MS-DOS. The 386 Translator, $395; with Intel 80386 chip, $895.

American Computer & Peripheral Inc, 2720 S Croddy Way, Santa Ana, CA 92704. Phone (714) 545-2004.

Circle No 399

I/O BOARD

- *Controls as many as 72 I/O lines*
- *Latches eight external interrupts*

The PC-XIO board allows you to set up and use an IBM PC or compatible computer to control and communicate with electrical apparatus and electronic instruments. The interface board can have as many as 72 discrete inputs or outputs (in groups of four) and as many as eight latchable interrupts. It provides direct local control of test equipment, assembly and inspection devices, robotics, process controls, and other instruments you select. Jumper wires select input and output lines in groups of four. Jumpers also let you connect as many as eight interrupt inputs to individual I/O points on the board. The manufacturer supplies software and documentation to support routines written in Microsoft Basic, Turbo Pascal, Lattice C, and 8088 assembly code. The documentation also includes concise examples and test programs. $445.

Step Control Ltd, 910 St Vincent Ave, Santa Barbara, CA 93101. Phone (805) 966-9553.

Circle No 400

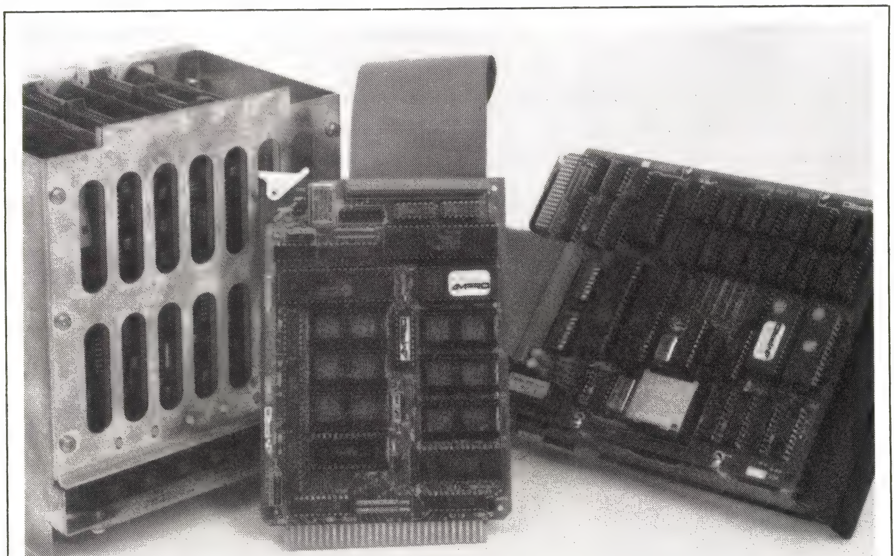
SCSI I/O PROCESSOR

- *Links I/O boards to SCSI ports*
- *Supports STD Bus peripherals*

The company's SCSI/IOP, an intelligent I/O processor, adds real-time control and measurement capabilities to computer systems that furnish a SCSI interface. The processor plugs into a normal STD Bus card cage and controls STD Bus I/O boards, such as A/D converters, video-display controllers, speech synthesizers, and network interfaces. To use the SCSI/IOP, you need a SCSI host adapter. (These low-cost adapters are available for many system architectures, including IBM PC, DEC, Multibus, and VME Bus architectures.) The SCSI bus arbitration allows as many as eight host computers and processors to share resources. The processor includes a 4- or 6-MHz Z80 µP, eight byte-wide memory sockets having as much as 64k bytes of EPROM/RAM, and a Z80-family counter/timer controller. An NCR 5380 SCSI protocol controller with ANSI X3T9.2 SCSI compatibility provides the interface to the SCSI bus. Basic firmware operations include reading and writing I/O-port data, creating and suspending tasks, and initializing the device. The processor implements the STD Bus's vectored-interrupt structure. It provides both the SCSI initiator and target functions, including the peer-to-peer message function. STD Bus SCSI/IOP with 4k bytes of EPROM and 2k bytes of RAM, $95 (100).

Ampro Computers Inc, Box 390427, Mountain View, CA 94039. Phone (415) 962-0230. TLX 4940302.

Circle No 401



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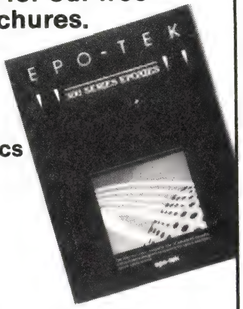

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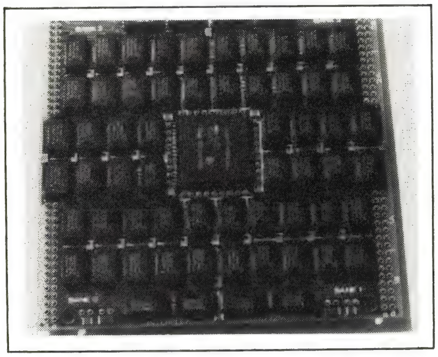


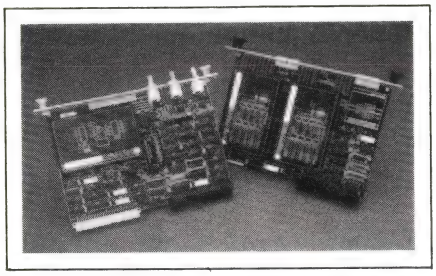
MEMORY/CONTROLLER

- *Furnishes either CMOS or NMOS dynamic RAM*
- *Consists of four layers*

The DM772M, a 2M-byte memory-and-controller module, uses all surface-mount components. Measuring 4.5×4.5 in, the 4-layer board uses interface connections similar to those in a pin-grid array. It contains four 256k-word×16-bit banks, which you address either by bytes or 16-bit words. The dynamic RAMs' input and output data pins have their own ports, and the module's CMOS THCT4502 controller has TTL/CMOS-compatible inputs. You can choose either NMOS or CMOS dynamic RAM. A board with 150-nsec dynamic RAM costs approximately $495 (100).

Interplex Inc, 742 Melville Ave, Palo Alto CA 94301. Phone (415) 325-5255.

Circle No 402



CONVERSION BOARDS

- *Provide both D/A- and A/D-conversion functions*
- *Offer 16-bit resolution*

The DT1407 analog-I/O board and the DT1403 D/A-converter board are available for VME Bus comput-

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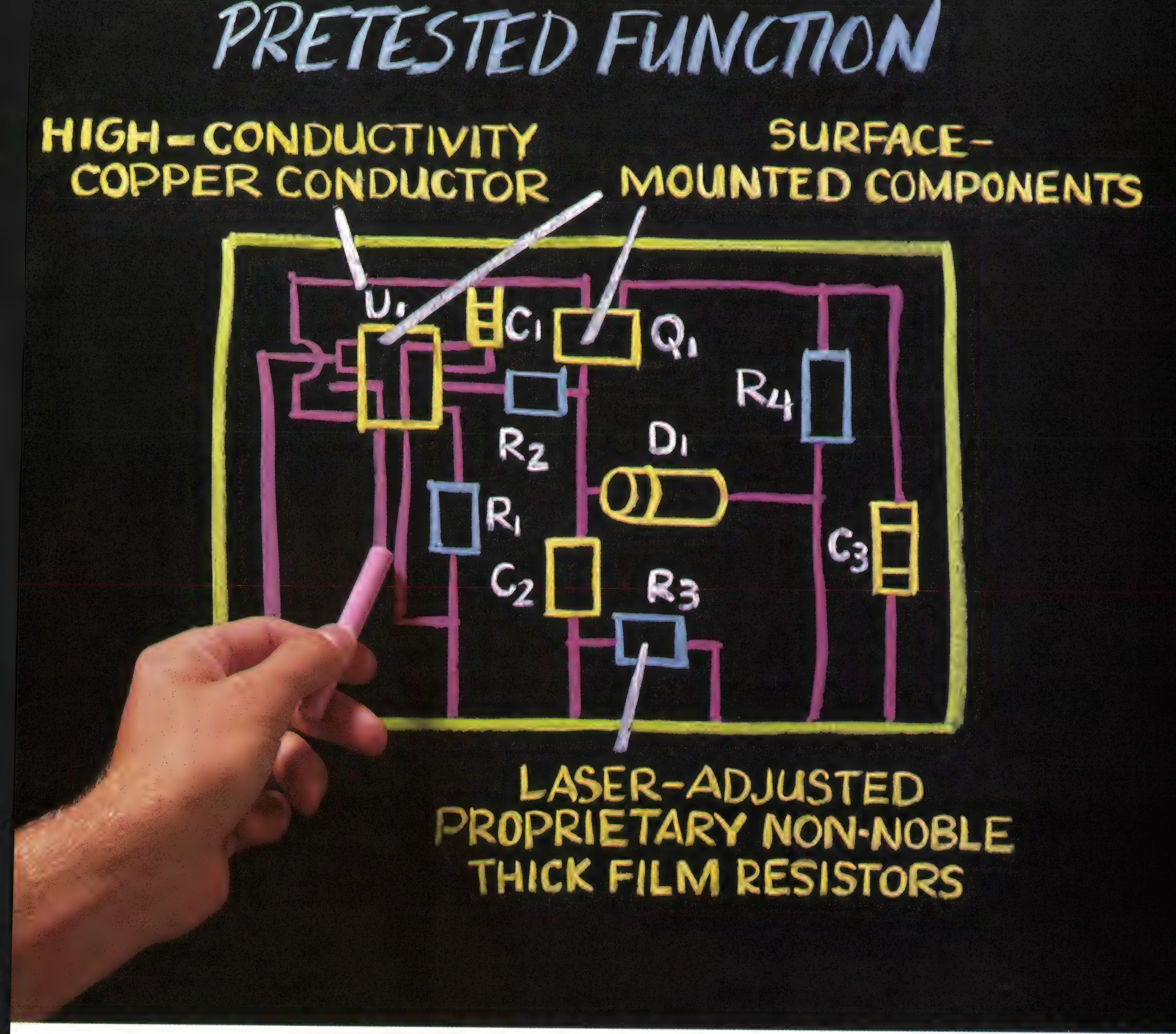
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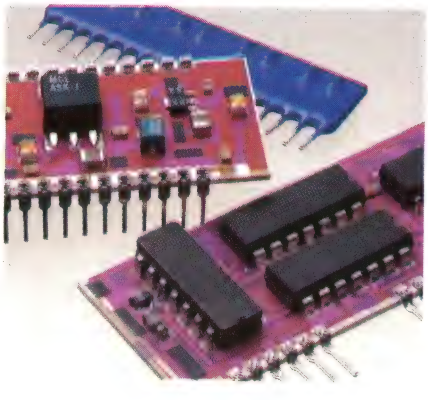

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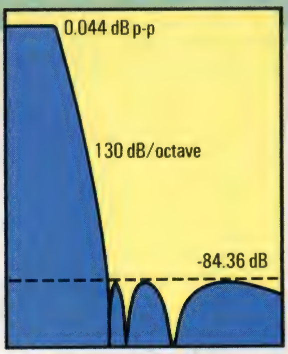

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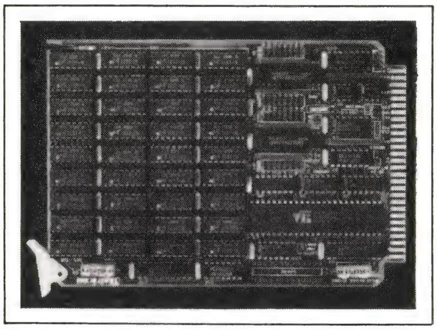
CIRCLE NO 146

ers. The DT1403 is the only 16-bit D/A-converter board currently available on the VME Bus, according to the manufacturer. The DT1407 has a 16-bit, 100-kHz A/D-converter subsystem with four differential inputs. It also includes two 12-bit, 125-kHz D/A converters, an onboard programmable clock (which can start A/D conversions or control off-board events), and 16 lines of digital I/O organized as two 8-line ports. The DT1403 D/A-converter board has two or four 16-bit D/A converters that have settling times of 10 μsec each (100-kHz throughput) and output ranges of ±10V. Glitch energy is guaranteed to be <½ LSB, and the deglitching circuit doesn't need any adjustments. The DT1407, DT1403-2, and DT1403-4 cost $2765, $1400, and $2095, respectively.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. TLX 951646.

Circle No 403



STD MEMORY BOARD

- *Offers range of addresses*
- *Includes power-fail detection, write protection, and refresh*

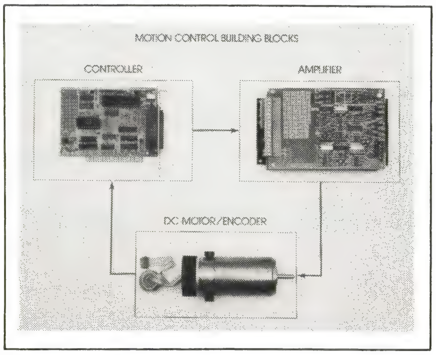
The MS-1DR, a 1M-byte dynamic-RAM module, has a jumper-selectable memory address space. You can define memory in 64k-byte increments and disable any 64k-byte memory block within the 1M-byte space. The board uses 20-bit addressing; total address range is expandable to 2M bytes. In addition, you can use four additional address lines, for a total of 24, to achieve a 16M-byte system. The module provides parity-error detection and offers a choice of three signals to notify your system that a single bit error has occurred. It also offers dc power-fail detection, write protection, and onboard refresh. A 1-year warranty is standard. Versions having less than 256k bytes, $795; 256k-, 512k-, and 768k-byte versions, $445, $545, and $645, respectively.

Datricon Corp, 16398 SW 72nd Ave, Portland, OR 97224. Phone (503) 684-3232. TWX 910-455-8184.

Circle No 404

MOTION CONTROLLER

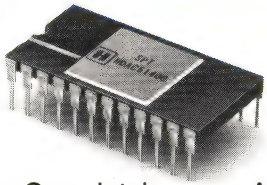
- *Available for IBM PC, RS-232C, VME, Multibus, and STD buses*
- *Interchangeable components include controller, motor, sensor*



You can form a motion-control system by selecting from BBS/Series boards, which include a motion controller, motor, feedback sensor, and amplifier. Motors are available in torque ranges from 5 to 500 oz-in. and with encoder resolutions as high as 1000 parts/revolution. You can select controllers that reside on the following buses: IBM PC, RS-232C, VME, Multibus, and STD. A pulse-input format is also available for applications requiring a direct interface to an indexer or pulse generator. Typical position accuracy at stop with no load is 0.18°. A PWM amplifier connects the controller and motor, generating continuous

THE WORLD'S FASTEST VIDEO DACs JUST GOT FASTER... 400 MWPS!

Our exciting new 8-bit raster DAC, the HDAC51400, operates at 400 MWPS* (typ.) conversion rate for truly superior graphics resolution.



☐ Completely "video-ready"
☐ ECL compatible
☐ Available in both a 24 lead CERDIP and ceramic sidebrazed DIP

*MWPS (Megawords Per Second) is the digital update rate.

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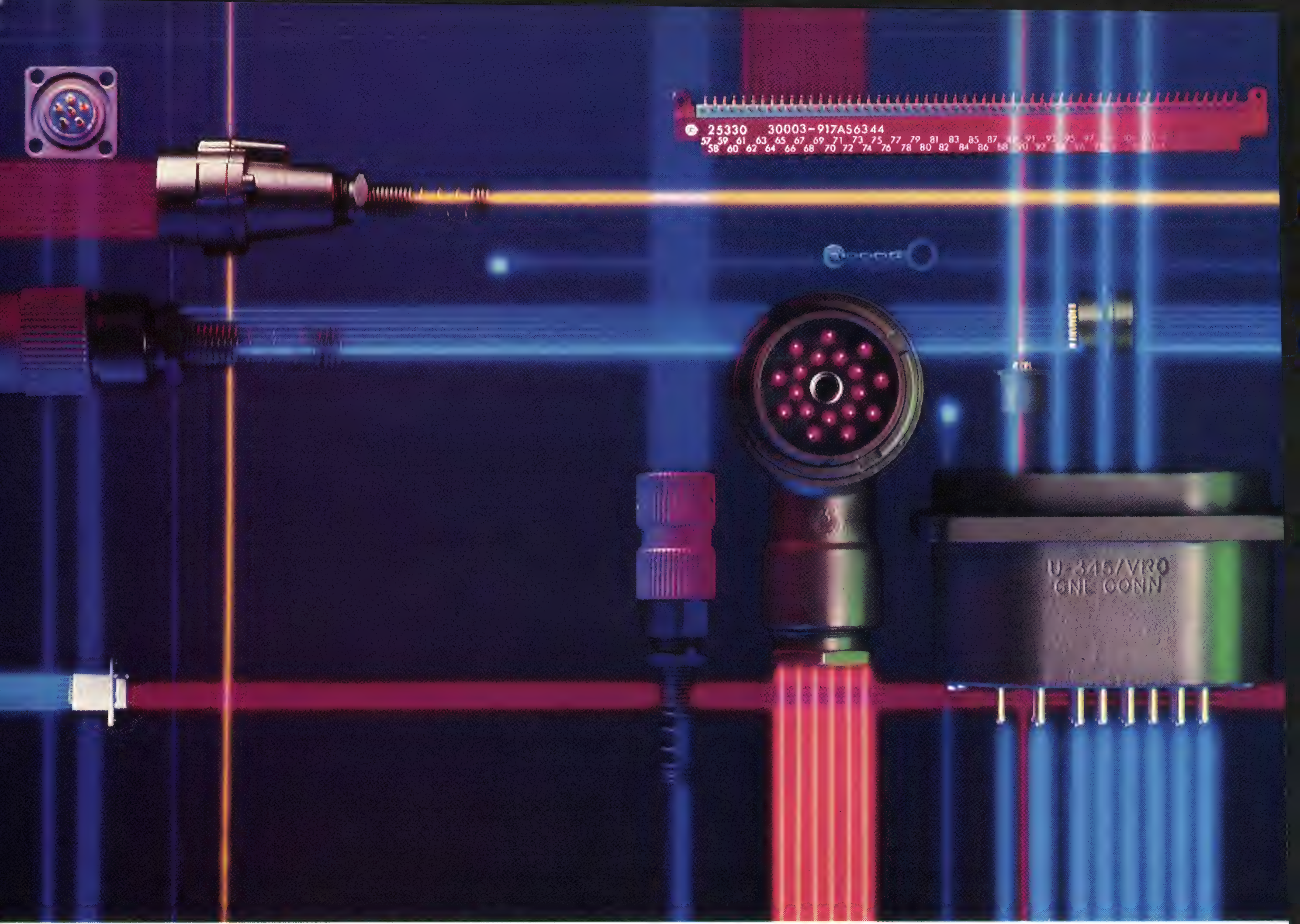


THE PAST, PRESENT AND FUTURE LEADER IN INTERCONNECTION SYSTEMS FOR TACTICAL COMMUNICATIONS.

Somewhere at this very second, information vital to our national security is safely passing through a GC connection device.

An obscure thought perhaps, but a reassuring one to design engineers who have been specifying GC connectors for a broad range of C³ applications for two decades.

In fact, our list of customers looks like the 'who's who' of the C³ world. Industry leaders that have come to rely on one of the leaders in reliability—General Connector.

#1 IN AUDIO,
POWER & U-TYPE CONNECTORS

A familiar face on many C³ devices for years has been the GC Audio connector. A real workhorse, this proven design is used primarily for reliable interconnection between hand/headsets and portable or fixed transceivers, the SINCGARS program for example.

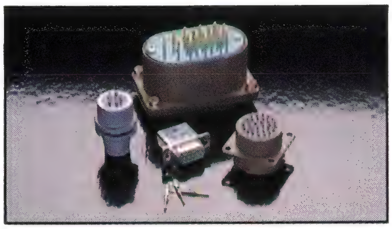
A familiar face, one of the popular GC Audio connectors.

Further, in Power and U-Type connectors, where GC is unsurpassed in the number of connectors now in use, GC leadership is evidenced by an extensive offering of standard connectors. And a broad list of custom capabilities—including filtering for EMI/RFI control.

CONNECTING WITH THE FUTURE

Few would argue with the assumption that tactical communications, in the next twenty years, will reach astounding new levels of complexity, as well as performance.

At General Connector, we believe that this geometric progression in technology will make the role of basic components like our connectors even more important. And you can expect us to live up to this responsibility. Reliably.



Filtered connectors—part of the GC custom capability.

For more information contact:
Richard W. Roberts, Product
Marketing Manager at
(617) 969-0920.

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Telephone: 617-244-5706
TWX: 710-335-6794
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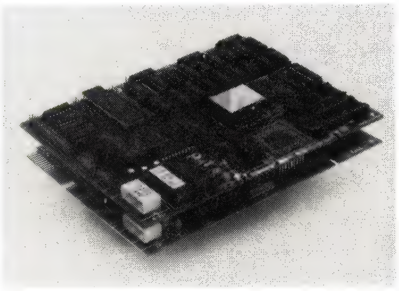
CIRCLE NO 148

current as high as 10A at 70V. Controller functions include point-to-point positioning, phase-lock speed control, velocity profiling, torque control, and homing; coordinated motion, nonvolatile memory, uncommitted I/O, and sequencing are optional. From $995.

Galil Motion Control, 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494.

Circle No 405



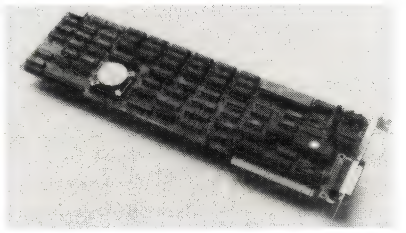
COMPUTER

- *Two-board μC measures 5.75×7.75×1 in.*
- *OS offers multitasking capabilities*

A 2-board microcomputer and a multitasking operating system together occupy nearly the same space as a half-height 5¼-in. disk drive. The 2-board set comprises the Little Board/186 single-board computer with an Expansion/186 daughter board. Measuring 5.75×7.75×1 in., the board set includes an 8-MHz 80186 CPU, 1M byte of RAM, 128k bytes of EPROM, four serial ports (RS-232C or RS-422), a floppy-disk controller, a SCSI bus interface, a printer port, an 8087 math coprocessor, a battery-backed real-time clock, an I/O expansion bus, and asynchronous or synchronous serial protocols. The multiuser operating system is Concurrent DOS 4.1 (Goodall Computer Systems, San Francisco, CA). You can use unmodified MS-DOS programs and many IBM PC applications that don't access video RAM or logic. Little Board/186 and Expansion/186 Board, $895; Concurrent DOS 4.1, $250 (2-user version), $300 (4-user version).

Ampro Computers Inc, Box 390427, Mountain View, CA 94039. Phone (415) 962-0230. TLX 4940302.

Circle No 406



COMM BOARD

- *Communicates to 800k bps*
- *Supports synchronous and asynchronous standards*

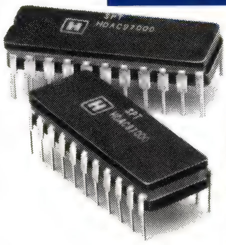
The WNIM-186, a coprocessor board for IBM PCs, PC/XTs, PC/ATs, and compatibles based on the 80186 μP, attains communications speeds as high as 800k bps. The board's transmission techniques include asynchronous, bisynchronous, X.25, and Systems Network Architecture and synchronous data-link control (SNA/SDLC) communications. The serial communications logic provides interfaces for two RS-232C, RS-422, or V.35 communications ports, each operating at speeds as high as 800k bps. The board incorporates an 8-MHz 80186 CPU and as much as 512k bytes of dual-ported memory with parity. Switches let you change the base addresses of onboard memory and I/O devices to avoid conflicts with other installed PC options. With 128k-byte memory, $695; with 512k-byte memory, $795.

Gateway Communications Inc, 16782 Red Hill Ave, Irvine, CA 92714. Phone (714) 261-0762.

Circle No 407

A SECOND SOURCE VIDEO DAC THAT'S TWICE AS FAST... 200 MWPS!

Go beyond Analog Devices' AD9700 with Honeywell Signal Processing Technologies' pin-compatible, high-speed, 8-bit HDAC97000 for truly superior video displays.



	Honeywell SPT	Analog Devices
Settling Time	10 ns to .2%	12 ns to .4%
Slew Rate	300 v/μs Min.	300 v/μs typ.
Conversion Rate	200 MWPS*	100 MWPS*
Rise/Fall Time	1.7 ns Max.	2 ns typ.

*MWPS (Megawords Per Second) is the digital update rate.

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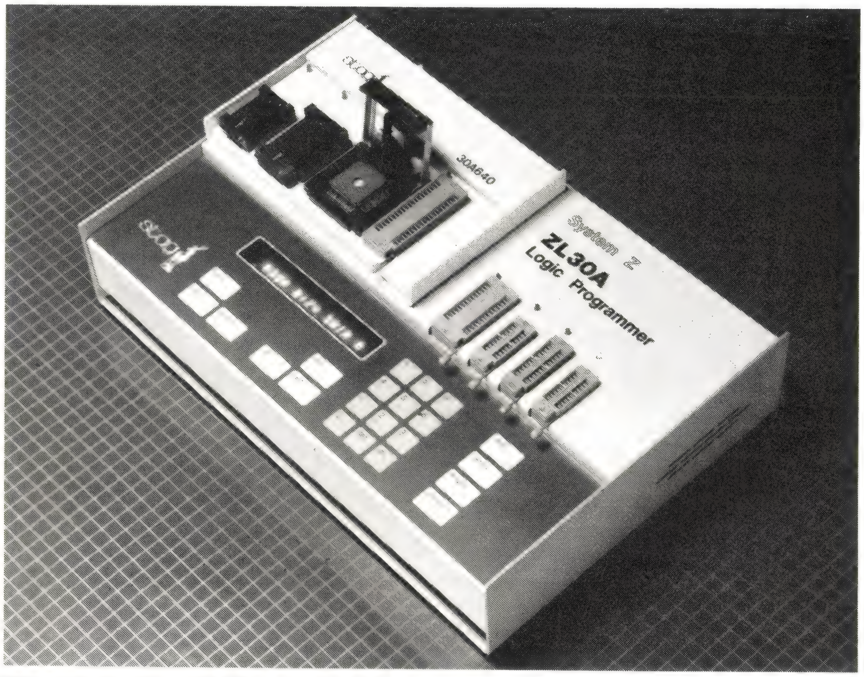
SMD PLD PROGRAMMER

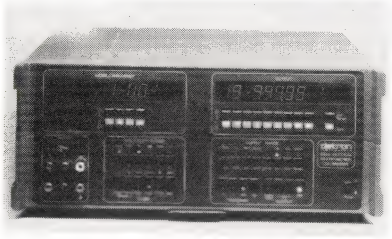
- *Features built-in ZIF sockets*
- *Provides stand-alone and remote-control operation*

The ZL30A programmer has built-in zero-insertion-force sockets for 20-, 24-, and 28-pin devices; it will accept optional adapter modules for surface-mounted devices. The instrument supports a range of programmable logic devices, including PAL, IFL, EPLD, and GAL. The device operates as a stand-alone unit or by remote control via an RS-232C or IEEE-488 interface. It can interface with common types of automatic device handlers. $3495.

Stag Microsystems, 528-5 Weddell Dr, Sunnyvale, CA 94086. Phone (408) 745-1991.

Circle No 408





DMM CALIBRATOR

- *Calibrates dc/ac voltage, dc/ac current*
- *Features self-calibration*

The Model 4700 Autocal DMM calibrator handles all digital voltmeters and multimeters having 6½-digit performance as well as analog instruments and other general-purpose test equipment. The device does not require an air-conditioned environment. The modular calibrator's capabilities include dc voltage (10 nV to 1100V), ac voltage (100 nV to 1100V), dc current (0.1 nA to 2A), ac current (0.1 nA to 2A), and resistance (10Ω to 100 MΩ). These outputs are generated from a single set of terminals, thus enabling hands-off calibration of multimeters when controlled via an IEEE bus. The instrument features IEEE-488 compatability and self-calibration. $9995 to $17,985. Delivery, 60 days ARO.

Datron Instruments, 4125 SW Martin Hwy, Stuart, FL 33497. Phone (800) 327-0938.

Circle No 409

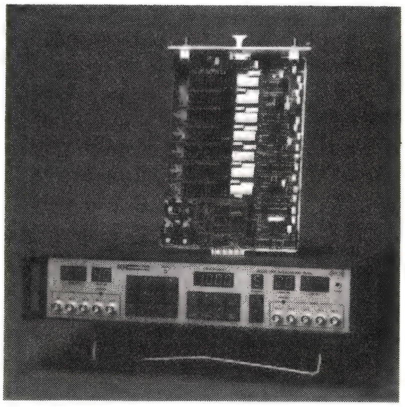
ELLIPTICAL FILTER

- *Exhibits <0.3-dB p-p passband ripple*
- *Features ac/dc coupling*

The Model 3905 programmable multichannel filter is a 5-channel elliptical filter. The device provides 115-dB/octave rolloff, <0.3-dB p-p passband ripple, and <100-μV output noise, in a lowpass or highpass configuration from 1 Hz to 99 kHz. Each channel has selectable I/O gain, ac/dc coupling, and variable cutoff frequency. You can program 80 complete 5-channel set-ups into nonvolatile memory. A complete system consists of control module and five plug-in filter modules in a 3½-in.-high mainframe. The mainframe provides indicators for I/O gain, cutoff-frequency programming, channel selection, power, and overload detection. Self-testing occurs at power-up. You can store and recall group settings with one command. $1750. Delivery, 90 days ARO.

Krohn-Hite Corp, Bodwell St, Avon, MA 02322. Phone (800) 582-1660; in MA, (617) 580-1660. TWX 710-345-0831.

Circle No 410



HONEYWELL SPT SETS THE PACE FOR HIGH RESOLUTION GRAPHICS!

The video display depicted is a graphic representation only.

Product	Resolution	Guaranteed Performance
HDAC34020	Triple 4-bit TTL Compatible	100 MWPS
HDAC10180B	8-bit	165 MWPS
HDAC10181B	8-bit w/reference	165 MWPS
HDAC34010	Triple 4-bit ECL Compatible	200 MWPS
HDAC97000	8-bit	200 MWPS
HDAC10180A	8-bit	275 MWPS
HDAC10181A	8-bit w/reference	275 MWPS
HDAC51400	8-bit w/reference	385 MWPS

MWPS (Megawords Per Second) is the digital update rate.

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Honeywell Signal Processing Technologies (SPT) brings you high-speed DAC technology that's easy to design-in without the need for additional costly parts.

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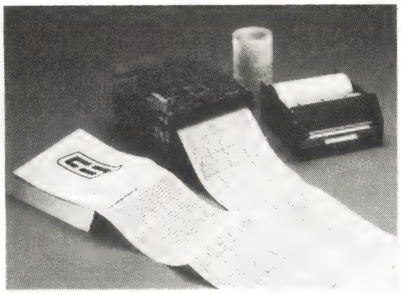


4-IN. RECORDER

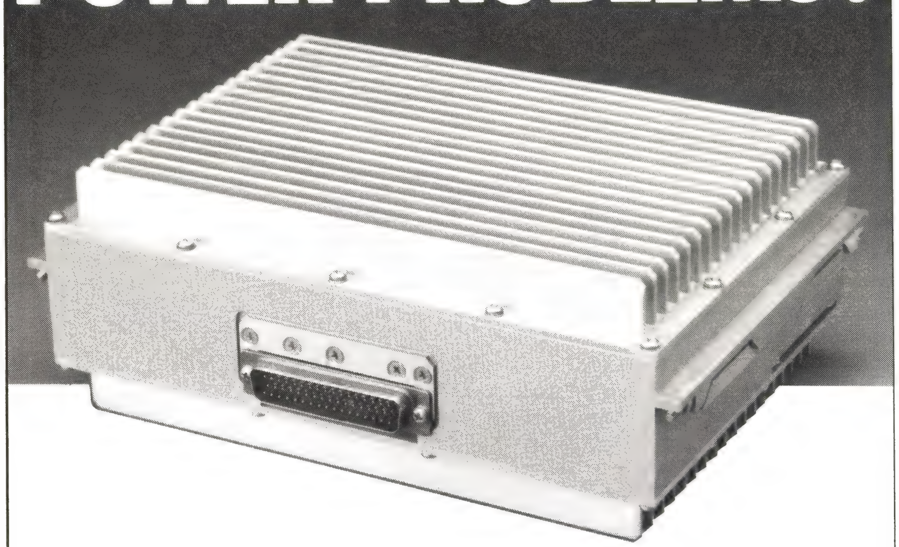
- *400- to 800-dot/in. resolution*
- *Fits 5¼-in. disk-drive slot*

The AR-100 4-in. thermal-array recorder has as many as four channels for analog input with a 10-bit dynamic range and resolution of 400 to 800 dots/in. (16 to 32 dots/mm). The device fits into the space of a 5¼-in. full-height disk drive. Because of its modular design, you can purchase the device with or without power supply, logic card, and analog-input option. The light-weight recorder can print graphics, trace data, real-time annotation, and programmable character sets. A character buffer enables you to repeat 4×6-in. formats of custom grids, photos, logos, alphanumeric annotation, or any combination of these symbols, both horizontally and vertically. When used to record and print trace data (digital or analog), the device applies proprietary, curve-smoothing algorithms to enhance waveform appearance. The vertical format has 52 columns of alphanumeric test characters; the horizontal format has 26 rows of characters. You can intermix vertical and horizontal characters as required. The device also permits bit-mapped graphics for high-definition black-on-white output. You can access any of the 832 print-head elements (200 dots/in.) in each print stripe. The device charts speeds from 1 mm/hour to 50 mm/sec. $1050.

General Scanning Inc, 500 Arsenal St, Watertown, MA 02172. Phone (617) 924-1010.

Circle No 411

POWER PROBLEMS?



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CIRCLE NO 151

DC/DC CONVERTERS

- *Have power density* $>10W/in^3$
- *>80% efficiency*

The PS-2805 and PS-2815 dc/dc hybrid converters have an efficiency

HP has something to say to oscilloscope users..
No. 1 in a series.

No. 1 in a series.

Explore HP Digitizing Oscilloscopes.

Digitizing architecture is making scopes easier to use, and more efficient.

The move toward digitizing architecture in oscilloscopes is on. New digitizing scopes are easier to use, and can dramatically boost measurement efficiency for engineers and technicians in many applications.

Simple instrument setup.

With the new HP 54000 series digitizing oscilloscopes, you get a stable display on the screen faster, even if other users have left the scope in an unfamiliar operating mode. You simply push the "autoscale" button on the front panel. Your signal is correctly displayed on the screen. It all happens automatically, in seconds.

You can also store front-panel setups in memory for later use...a convenient feature, especially if your application calls for repeating several different instrument setups, or if the scope is shared by many users.

Automatic answers.

With conventional scopes, making measurements such as risetime or frequency is typically a lengthy process, involving manual calculations. With the HP 54000 series, you can make these measurements, and many more, automatically. That's because they are computed for you at the touch of a button from digitized information.

Instant hardcopy output.

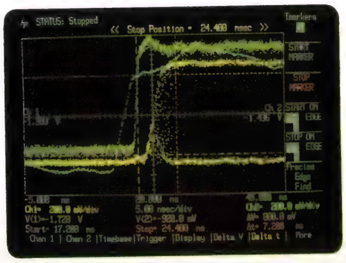
If you've ever fussed with oscilloscope cameras trying to photograph traces, you'll appreciate the digitizing difference. You simply push a button on the front panel of the HP 54000 series to get hardcopy of the waveform of interest, or scope setup, on HP graphic printers, or plotters.

No more grease pencils.

Unlike their conventional analog counterparts, digitizing oscilloscopes can store waveforms in memory. So you can call them up for later reference, or compare them on the display with "live" waveforms, without parallax. Traces remain clear and sharp, so you can make accurate measurements without time limits, even on stored and recalled traces.

Multiple colors enhance scope functionality.

Multiple, selectable display colors let you distinguish overlapping traces more easily. Associate waveforms with corresponding measurement and setup data. Emphasize special conditions, such as the color red indicating when measured data is outside of control limits. And tailor the system to your own way of working—to improve contrast or aid recognition, for example. Functional color is available on the HP 54110D digitizing oscilloscope.



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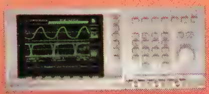
*Offer expires Dec. 31, 1986.



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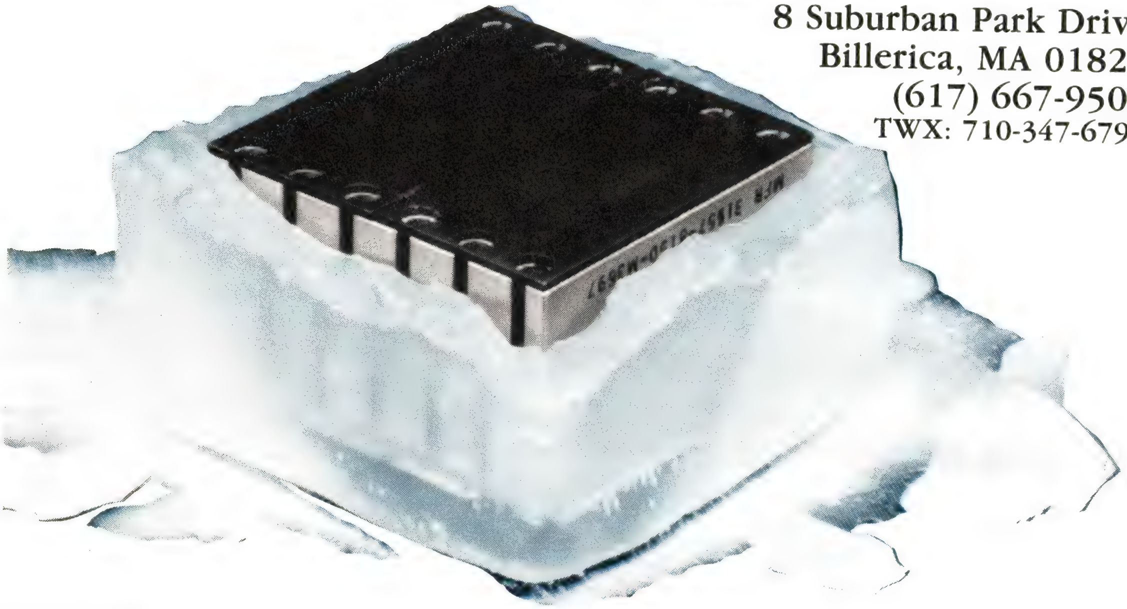


CIRCLE NO 152

rating of greater than 80%. Power density is >10W/in^3 with no external heat sinks or convection cooling needed. The PS-2805 produces an isolated, 5W, 5V dc output from a 28V dc input. The 7.5W PS-2815 produces a ±15V dc multiple output from a 28V dc input. The devices have short-circuit protection with an automatic reset. The converters also feature external shutdown control. Both models come in packages that measure <0.75 in^3. The devices operate over −55 to +100°C with 0 to 200 μF of load capacitance. PS-2805, $352; PS-2815, $462.

Intech Inc, Microcircuits Div, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930.

Circle No 412

300W SWITCHERS

- *Offer 80% efficiency*
- *UL, CSA approved*

The V300 Series switchers are UL and CSA approved. They deliver 5V at 40A on the main output and various combinations of ±12, ±15, −5, and 24V on auxiliary outputs. The devices feature 2.8W/in^3 power density, 80-kHz conversion frequency, 80% efficiency typ, 3750V ac isolation, 8-mm safety spacing, and adherence to worldwide safety and EMI regulations. The 4-output units also feature optional current sharing and parallel operation without use of diodes; overvoltage protection on all auxiliaries; power-fail monitor; TTL-level inhibit input; and thermal shutdown. $223. Delivery, eight weeks ARO.

Deltron Inc, Box 1369, North Wales, PA 19454. Phone (215) 699-9261. TWX 510-661-8061.

Circle No 413

68020 EMULATOR

- *14-MHz real-time operation*
- *Performs symbolic debugging*

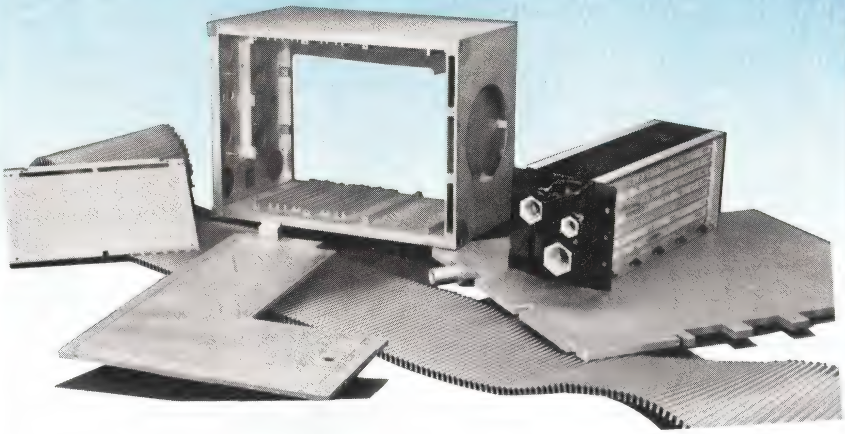
The MICE-32/68020, a 32-bit μP emulator, executes commands for system configuration, memory interface, I/O interface, register access, selective trace, breakpoint, and disassembly. The device can emulate in real time at clock speeds as fast as 14 MHz with no wait states. The unit performs symbolic debugging, memory mapping, logic-state analysis, and software-performance analysis. The 104-bit-wide trace memory records address data, machine status, and interval or elapsed-time stamping. The 256k bytes of emulation memory can be located anywhere within the μP's 4G-byte memory space. $12,000.

New Micro Inc, 16901 S Western Ave, Gardena, CA 90247. Phone (213) 538-5369.

Circle No 414

FROM DESIGN TO DELIVERY...

THE LEADER IN MILITARY AIRBORNE/SHIPBOARD COMPUTER ENCLOSURES



Lockhart manufactures custom airborne/shipboard computer enclosures, providing both equipment mounting and cooling structures for military electronic systems. Lockhart computer enclosures are manufactured of wrought aluminum construction for light weight and high strength, and assembled by fluxless vacuum brazing or aluminum salt bath brazing.

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CIRCLE NO 153

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10 W
REGULATED POWER SUPPLY
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+ INPUT −
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RON WALKER
Principal Engineer

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3	5-28	3-5K
6	28	5-5K
10	28	5-5K
25, 50	28, 48	5-48
100, 150	28, 48	5-48

Typical Tecnetics AC/DC Power Supplies

WATTS	INPUT VAC/Hz/Φ	OUTPUT VDC
3, 6	115/400/1	5-28
10, 15, 20	115/400/1	5-28
25, 50	115/400/3, 1	5-48
100	115/400/3, 1	5-48
200	115/47-440/3	5-48
1000	115/400/3	28

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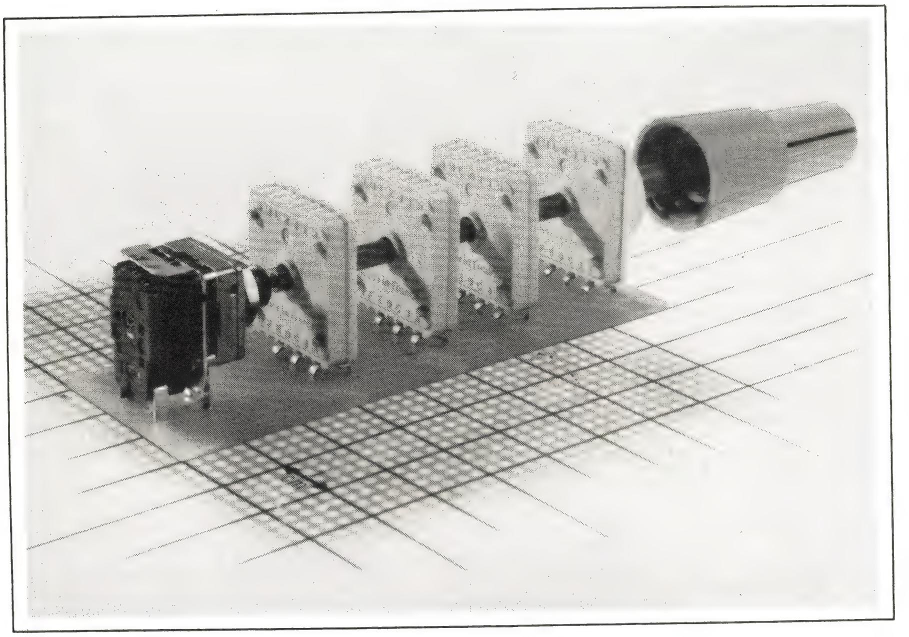
CIRCLE NO 154



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- *Available in 10-, 12-, and 16-way versions*
- *Rotates 360°*

RTA-H Series rotary switches are suitable for horizontal mounting on a single pc board or for sandwiching between two pc boards. The distance between the horizontal shaft and the pc board is 15 mm. The 360°-rotation switches are available in single-pole, 10-way, 12-way, or 16-way versions, or as 16-way true- or complementary-output binary-coded versions. End stops to limit rotation of the switch are optional. Switch operation can be make-before-break or break-before-make, and the switches are available in either silver- or gold-contact versions. The silver contacts switch a maximum of 250 mA and have a switching-power rating of 5 VA. The gold contacts switch a maximum current of 100 mA and have a switching-power rating of 1 VA. Both types can carry a current of 1A. The life expectancy of the contacts at rated switching power is 10,000 operations, and contact resistance after endurance testing is less than 150 mΩ. Switch wafers are mobile along the operating shaft for ease of assembly. The assembly is also available with a hollow shaft, which allows you to mount a concentric potentiometer or switch assembly. Fr fr 15 (100) for a single-wafer version; Fr fr 10 per additional wafer.

ITT Commutateurs et Relais, 157 rue des Blains, F92220 Bagneux, France. Phone 46658555. TLX 260712.

Circle No 415

LOCAL-BUS ARBITER

- *Arbitrates bus access for μP and three peripherals*
- *Assigns three interrupt priorities*

The SAB 82200 bus arbiter IC allows you to arbitrate access to a μP system's local bus for as many as four devices—three peripheral devices and the μP. Alternatively, you can use it to assign priorities to as many as three interrupt sources. The arbiter accepts a bus- or interrupt-request input from each of the three peripheral devices and passes the input to the μP using a programmable priority pattern. It then returns the μP's bus- or interrupt-acknowledge signal to the relevant peripheral device. The SAB 82200 comes in a 22-pin DIP. DM 27 (100).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 416

Siemens Components Inc, 186 Wood Ave S, Iselin, NJ 08830. Phone (201) 321-3400.

Circle No 417

STATIC RAM

- *Specs 25- or 35-nsec access times*
- *Processed to MIL-STD-883C*

The MKB41H68 is a 4k×4-bit, TTL-compatible CMOS static RAM processed to MIL-STD-883, Class B, Revision C requirements. The device is available in two versions, which have respective address-access times of 25 or 35 nsec. The RAMs spec a cycle time equal to the address-access time. A 2-stage power-down mode reduces maximum operating current to 6 mA when the chip-enable input is driven to a TTL high level. The power-down mode reduces the current to 500 μA max when you drive the chip-enable input to the level of the power supply. The RAMs operate from a 5V±10% supply and have an operating case-temperature range of −55 to +125°C. They are available in 20-pin, JEDEC-standard ceramic DIPs, ceramic LCCs, or ceramic flat packs. $45 (100).

Thomson Semiconducteurs, 45 Ave de l'Europe, 78140 Velizy, France. Phone (33) (3) 9469719. TLX 204780.

Circle No 418

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000. TLX 370643.

Circle No 419

SIGNAL PROCESSOR

- *Adds 10 parallel signal inputs*
- *Uses analog CCD shift registers*

You can use the WA1001 signal-processing IC for infrared imaging, sonar and radar beam forming, analog transversal filtering, and similar applications. The device allows you to add together as many as 10 parallel inputs; each signal is delayed with respect to the previous input by six periods referenced to the input clock. To delay the input signals with respect to each other, the IC uses analog CCD shift registers between the signal inputs. You can thus control the delay period with a single TTL-compatible external clock, which you can operate at frequencies as high as 15 MHz. A bias input allows you to provide dc bias to ac-coupled inputs, and an on-chip voltage generator provides a reference voltage for each input's buffer amplifier. You can override the on-chip reference voltage with an external reference. An S/H amplifier on the device output generates a continuous analog-output waveform with a maximum amplitude of 4V p-p and a dynamic range of 87 dB typ (85 dB min). A digital gain-control input allows you to alter the gain between fixed gain limits of −6.6 and −9.1 dB typ. The device requires a 15 and a −5V supply and operates over 0 to 70°C. It's available in a 24-pin ceramic DIP or a 24-pin LCC. $64 (1000).

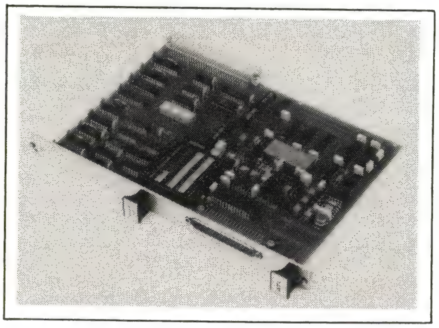
Walmsley Microsystems Ltd, Aston Science Pk, Love Lane, Birmingham B7 4BJ, UK. Phone (021) 359-0981. TLX 334535.

Circle No 434

VME BUS A/D CARDS

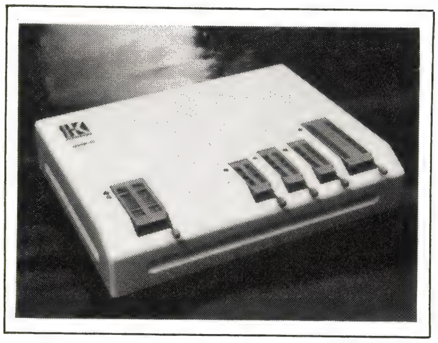
- *Have 12-bit A/D-converter resolution*
- *Analog input channels are individually programmable*

The AD12VME-16 and -32 VME Bus A/D converter cards provide you with 16 or 32 analog input channels, respectively. You can configure each pair of input channels either as two single-ended inputs or as one differential input. Each input channel is individually software programmable for single-ended or differential operation, for unipolar- or bipolar-input capability, and for any full-scale range between 100 mV and ±10V. The board has 12-bit resolution, an overall system accuracy of 0.024% on all input ranges, and a maximum throughput rate of 28k samples/sec. It also provides 500V isolation between the input and VME Bus grounds. AD12VME-16, £1395; AD12VME-32, £1520.



Anglia Technology Ltd, University Village, University of East Anglia, Norwich, Norfolk NR4 7TJ, UK. Phone (0603) 503057. TLX 975646.

Circle No 435



ADAPTERS

- *Adapters let you program 40-pin, 1M-bit EPROM*
- *Module programs 1M-bit EPROM in less than 4 minutes*

The 40-pin SA-48 and PA-48 adapters allow the company's MDM MOS-device module and the UPM/C universal test and programming module, respectively, to program the 40-pin, 1M-bit AMD-27C1024 EPROM. MDM modules with at least software revision 3.0, and all UPM/C modules, accept the adapters without modification. MDM modules with software revisions earlier than revision 3.0 require updating before they can accept the adapters. You can program 27C1024 EPROMs on the MDM and UPM/C modules, fitted with the adapters, in 5 minutes and 3 minutes, 15 sec, respectively. SA-48, approximately $140; PA-48, approximately $220.

Kontron Messtechnik GmbH, Oskar-von-Miller-Strasse 1, 8057 Eching/Munich, West Germany. Phone (08165) 77309. TLX 526719.

Circle No 436

Kontron Electronic Inc, 630 Price Ave, Redwood City, CA 94063. Phone (415) 361-1012.

Circle No 439

PRINTER

- *Operates to 400 characters/sec*
- *Offers wide range of character fonts*

The Model 3/1 18-needle dot-matrix printer produces 400 characters/sec in normal mode and 100 characters/sec in its 2-pass, near-letter-quality (NLQ) mode. The unit features an encapsulated print head and a paper-feed mechanism that minimizes noise. The unit incorporates five standard character fonts; additional fonts come in optional plug-in cassettes. You can also download character sets to the printer to produce hard-copy graphics. The printer simultaneously accepts a tractor-feed option and an automatic, single- or double-bin cut-sheet feeder option. You can feed in cut sheets by hand while the tractor feed is in position. A color printing option is also available. SFr 5950.

Wenger Printers AG, 23-25 Im Kagen, 4153 Reinach, Switzerland. Phone (061) 768787. TLX 967048.

Circle No 437

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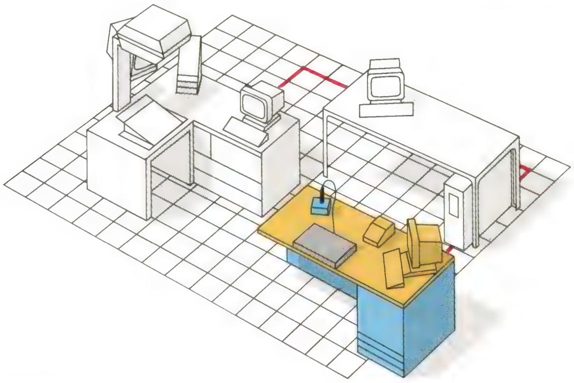

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CIRCLE NO 156

INTERNATIONAL

PROTOCOL ANALYZER

- *Operates at data rates as high as 64k bps*
- *Includes RS-232C/V.24 and RS-449/V.36 interfaces*

The TE707 is an analyzer and signal-unit simulator for testing communications equipment that uses the CCITT System 7 common-channel signaling protocol. In its analysis mode, the TE707 operates as a full-duplex analyzer for data rates as high as 64k bps. It analyzes signal-unit sequencing and control, and it performs selective message acquisition, event analysis, and clock-controlled logging of signal-unit data. You can display data traffic in a split-screen, full-duplex, time-correlated mode; each side of the transmission is displayed in CCITT-7 mnemonics or hexadecimal code. You can store recorded data on the unit's integral 3½-in., 350k-byte disk drives. In its signal-unit-generation/simulation mode, the TE707 transmits stored signal units that are linked to make up test messages. The unit includes RS-232C/V.24 and RS-449/V.36 interfaces. $25,000.

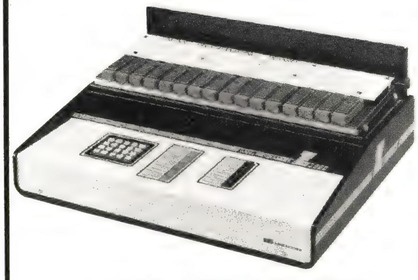
Tekelec Airtronic, rue Carle Vernet, 92310 Sevres, France. Phone (14) 5347535. TLX 204552.

Circle No 420

Tekelec, 26540 Agoura Rd, Calabasas, CA 91302. Phone (818) 880-5656.

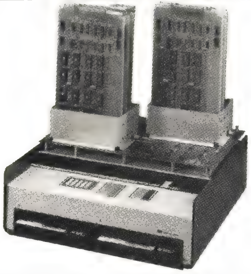
Circle No 438

AMERICA'S BEST PROGRAMMERS



Z-3000 HIGH VOLUME GANG/SET PROGRAMMER

- 14,000 27256s programmed per day.
- 32 EPROMs simultaneously with 1 to 8 DATA BLOCKS.
- 16 Intel or Motorola MCUs at a time.
- 64K to 256K bytes of DATA RAM.
- Simple one key programming operation.
- Two RS-232 ports with data transfer formats included.



Z-2500B IN-CIRCUIT MEMORY CARD PROGRAMMER

- Programs up to 32 memory cards with EPROMs or microcomputers at a time.
- Two 1.2 Mbyte DSDD floppy disk drives. Optional 20 Mbyte hard disk.
- Turnkey systems include programmer, terminal, custom interface hardware and software.
- Simple menu driven operation.

Z-1000B UNIVERSAL PROGRAMMER

- Over 600 PLDs, EPROMs, EEPROMs, bipolar PROMs and INTEL MCUs.
- Upgradeable PROM based software.
- Stand alone or PC/XT/AT operation.
- Two independent RS-232 ports.
- 64K or 256K bytes of DATA RAM.
- EXATRON handler interface is standard.

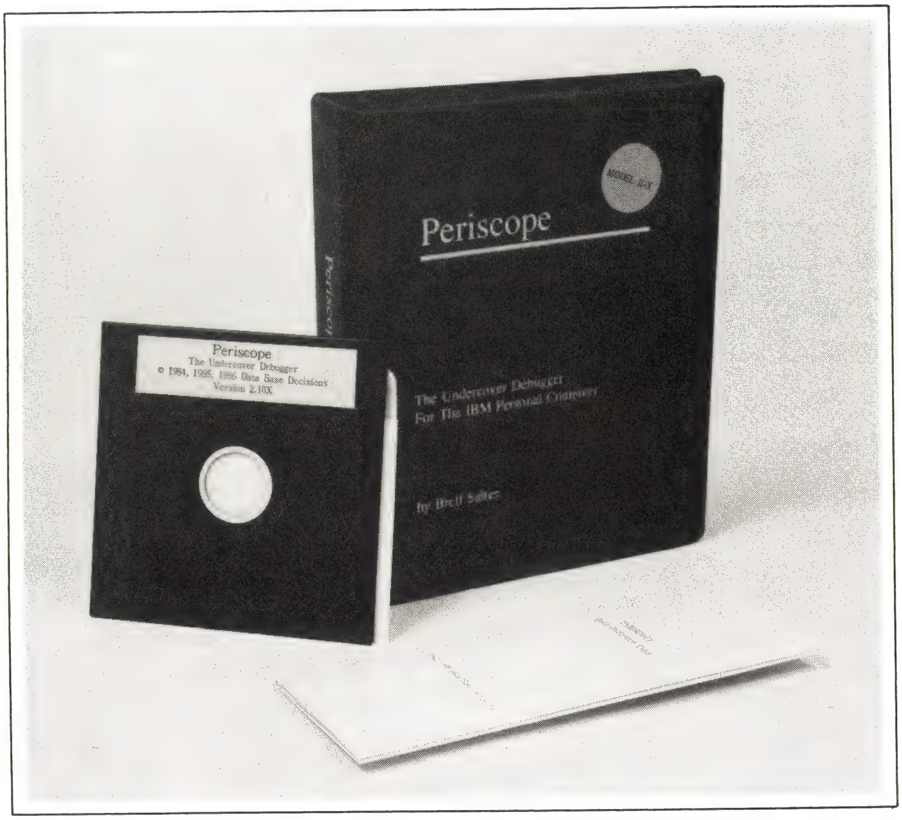
Z-1200B TWELVE SOCKET GANG/SET PROGRAMMER

- 2716-27512, 1 to 4 DATA BLOCKS.
- 64K to 256K bytes of DATA RAM.
- Software personality. No plug-ins.

ZAP SERIES low cost programmers for EPROMs and single-chip MCUs.

Z-400 for bipolar PROMs and EPROMs.

SUNRISE ELECTRONICS, INC.
524 South Vermont Avenue
Glendora, California 91740
(818) 914-1926


Periscope
MODEL II-X
The Undercover Debugger For The IBM Personal Computer
by Brett Salter
Periscope
The Undercover Debugger
© 1984, 1985, 1986 Data Base Decisions
Version 2.10X

DEBUGGING SYSTEM

- *Runs without protected-RAM board*
- *Lets you define as many as four data windows*

Periscope II-X, which runs on the IBM PC convertible, as well as on the PC, PC/XT, PC/AT, and compatibles, is an entry-level, software-only model of the Periscope debugger. (It doesn't include the protected RAM board and the break-out switch that come with earlier versions.) This version has accelerated monitor breakpoints; it's easier to use than other versions because its command-editing function is similar to DOSedit. The software works with 8087 and 80287 math coprocessors, Aztec and DeSmet C compilers, and 80286 coprocessor boards. It lets you trace back through executed commands. You can load multiple symbol tables and define as many as four data windows, and you can duplicate the program's output on a disk file and exit to DOS from the program. This version of the program also includes text-file viewing, expression evaluation, and enhanced comprehensive symbol support. $115.

Data Base Decisions, 14 Bonnie Lane, Atlanta, GA 30328. Phone (800) 722-7006; in GA, (404) 256-3860.

Circle No 422

SDLC FOR PCs

- *Allows PCs to exchange files at 9600 bps*
- *Lets you issue local PC-DOS commands to unattended PC*

Using IBM's SDLC (synchronous data-link control) protocol, Synctalk allows two IBM PCs to communicate and exchange files at speeds as high as 9600 bps. A menu-driven interface, similar to those found on asynchronous communications pack-

CIRCLE NO 184

The Subscriber Line Interface Circuit

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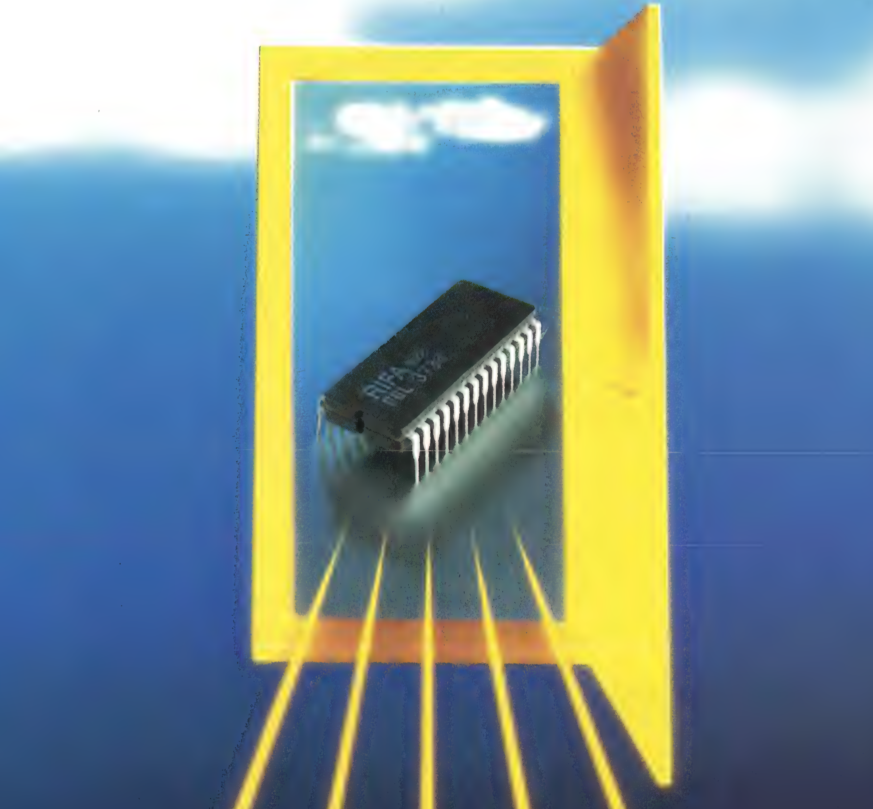

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CIRCLE NO 168

ages, allows either PC to initiate and control the exchange; both PCs must run the same version of the software. The package allows you to exchange messages interactively or transfer files with another attended PC; you can also issue local PC-DOS commands for execution by a remote, unattended PC. You can compress data on all transmissions and operate the software over both leased and dialed lines. An idle timer lets you avoid unnecessary line costs. Detailed help screens, password protection, and optional automatic-dialing and call-directory features also come with the package. To use the software, you need an IBM PC, PC/XT, PC/AT, or compatible computer equipped with at least 256k bytes of memory, an IBM SDLC adapter board, and a synchronous modem. $195.

Network Software Associates Inc, 22982 Mill Creek, Laguna Hills, CA 92653. Phone (714) 768-4013.

Circle No 423

DIAGNOSTIC TEST

- *Checks the full 80286 instruction set*
- *Tests all hardware components of IBM PC/ATs and compatibles*

The PC/AT Service Diagnostics software package tests all the hardware components of IBM PC/ATs and compatibles. The primary diagnostic routines test for correct operation of the 80286 CPU's instruction set (in both the compatibility and the protected modes) and the 80287 math coprocessor's instruction set. One test checks all memory existing within the full 16M-byte address space of the 80286. Other routines test the remaining mother-board components: the DMA controllers, the 8259 interrupt controller, the timer, and the real-time clock. The diagnostics also test all display adapters (including the enhanced graphics adapter), the keyboard controller, and the PC/AT keyboard. One disk routine checks the PC/AT's 1.2M-byte disk drive and 360k-byte drive for correct alignment. $225.

Supersoft, Box 1628, Champaign, IL 61820. Phone (800) 762-6629. TLX 270365.

Circle No 424

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DISK UTILITY

- *Features multiple, tree-structured directories*
- *Lets you select files by date or by project*

The SDF200 (structured directory format) is a hierarchical disk directory for use with the Basic 3.01/4.0 and Pascal 3.0/3.1 operating systems for HP Series 200/300 desktop computers. The directory's format is identical to the format used by the HP's SRM (shared resource manager) controller and Series 500 disks, but you don't need the SRM hardware. The directory files don't require contiguous space on the disk, so you don't have to repack the disk before creating a large file. This utility features multiple, tree-structured directories; logical file groupings; and 16-character file names. In addition, the utility automatically manages noncontiguous files and can extend files to the limit of available disk space. The selective backup feature allows you to copy only those files changed since a specific date, or just the files in the subsidiary tree associated with a particular project. $600.

Structured Software Systems Inc, 1072 Irick Rd, Mount Holly, NJ 08060. Phone (609) 267-1616.

Circle No 425

FILE UTILITY

- *Combines many standard file-manipulation functions*
- *Lets you scroll display forward, move from page to page*

Catalogue is a function-key-driven utility that operates on Burroughs and Convergent Technologies workstations running under the BTOS (Burroughs) or CTOS (Convergent Technologies) operating systems. It consists of a combination of many standard file-manipulation functions. The Delete, Copy, and Rename functions, as well as the Type and File functions, perform in the same way as the BTOS/CTOS functions of the same name. However, the utility lets you scroll the dump or type display forward and backward by using the Scroll Up/Down key; you can move from page to page as well by using the Next/Prev Page key. The Files function accepts information for building a new list of files, and you can use the standard field-editing capabilities. You can also sort or re-sort the list of files by name, size, or date/time of last modification. The package requires approximately 55k bytes of memory. If the file list is too long for the available memory, the program displays a warning. $189 per workstation or $289 per site.

CA Electronics, 640 Lancaster Ave, Frazer, PA 19355. Phone (215) 296-7190.

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IP1526	LM123	ULS2074-2077
IP1526A	IP123A	ULS2801-2805
IP1527A	LM137/137HV	ULS2811-2815
IP1543	IP137A/137AHV	ULS2821-2825
IP1544	LM138	
IP1842	IP138A	
IP1843	LM140/IP7800	
IP5560	IP140A/IP7800A	
IP5561	LM150	
IP35060A	IP150A	
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IP1P00	IP78M00A	
IP1P01	IP79M00	
IP1P125	IP79M00A	

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CIRCLE NO 158

SYSTEM V FOR PC/AT

- *Adaptation of Unix System V.2*
- *Enhancements include virtual-screen windows*

System V/AT is an adaptation of AT&T's Unix System V, Release 2 iAPX286 Version 1a; it turns a PC/AT or compatible computer into a multiuser, multitasking computer. The operating system has a number of features not found on other Unix implementations. For example, it includes Multiconsole, a virtual-screen windowing system; a dynamic disk buffer that improves RAM-disk performance; file-system hardening, which prevents data loss in case of a power failure; and several programs from the University of California at Berkeley. It also has record locking and read/write utilities for DOS disks, and it comes with Fortran 77 and large-model C compilers, as well as a symbolic debugger. The system is compatible (at the binary level) with the AT&T PC 6300 Plus Unix operating system. When versions for the 80286 and 80386 of AT&T's Unix System V Release 3 become available, therefore, the company will be able to upgrade System V/AT quickly to the same level. Run-time system, \$159; software-development system, \$169; text-processing system, \$169; complete package, \$439.

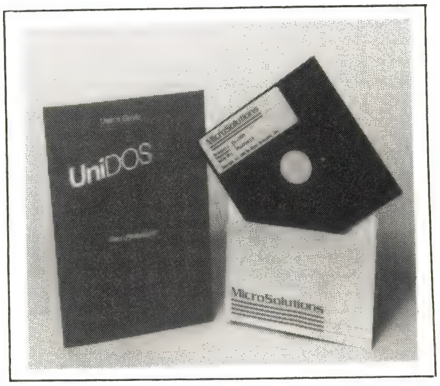
Microport Systems, 10096 Soquel Dr, Aptos, CA 95003. Phone (408) 688-0286.

Circle No 430

EMULATOR PROGRAM

- *Runs CP/M-80 programs on IBM PC*
- *Mixes DOS and CP/M programs on the same DOS disk*

UniDOS lets you run 8-bit CP/M programs directly on IBM PCs and compatibles without additional hardware. Emulating a Z80 μP, UniDOS can create a complete CP/M Version 2.2 environment. It executes Z80 instructions, so it doesn't require any changes to CP/M programs: You can run a CP/M program from DOS just by typing the program's name. CP/M programs can coexist with DOS programs on the same disk. If you also have UniForm, the vendor's format translator, you can insert a CP/M disk into your PC and run programs from the CP/M disk. UniDOS automatically senses the presence of an NEC V-Series μP in your PC. This μP can directly execute 8080 instructions, so it increases the execution speed of CP/M programs that use only 8080 instructions. However, UniDOS software must emulate Z80 instructions. \$69.95.



MicroSolutions Inc, 125 S Fourth St, DeKalb, IL 60115. Phone (815) 756-3411.

Circle No 431

EXPANDED MEMORY

- *Lets you perform multiple tasks concurrently*
- *Runs applications that require expanded memory*

The Concurrent PC DOS XM (expanded memory) operating system utilizes the AST/Quadram/Ashton-Tate enhanced expanded memory specification (AQA EEMS) to run multiple DOS sessions concurrently. It can also use the Lotus/Intel Microsoft expanded memory specification (LIM EMS) to run applications that require expanded memory. The system can run popular applications, such as Lotus 1-2-3, the dBase series, and Wordstar. According to the manufacturer, the operating system can run existing applications written for PC-DOS, MS-DOS, Concurrent DOS, and CP/M-86 without modification; it can also be upgraded for use with protected-mode 80286-based systems. You can perform multiple tasks concurrently, displaying background tasks either by switching screens or by using multiple windows. By adding the vendor's Gem (graphics environment manager), you can use a variety of graphics functions and application programs. The operating system comes with a configurable memory system, a menu-driven file manager, integrated on-line help, and accessory products that include a name-and-address filer, text editor, and print-spooling program. \$395.

Digital Research Inc, Box DRI, Monterey, CA 93942. Phone (408) 649-3896. TWX 910-360-5001.

Circle No 432

8051 C COMPILER

- *Provides full pointer support for all 8051 memory spaces*
- *Features run-time exception checking*

Micro/C-51 is a C language compiler for the 8051 family of single-chip μPs. It is a partial implementation of the C language as documented in *The C Programming Language* by Kernighan and Ritchie. In addition to full pointer support for all 8051 memory spaces, the device provides run-time exception checking of math and memory-access operations. It can access 250 local or remote devices. The compiler is available for 8051, 8052, and 8044 single-chip μCs. Operating under MS-DOS, it requires one drive and 256k bytes of memory. \$1495.

Micro Computer Control, Box 275, Hopewell, NJ 08525. Phone (609) 466-1751.

Circle No 433

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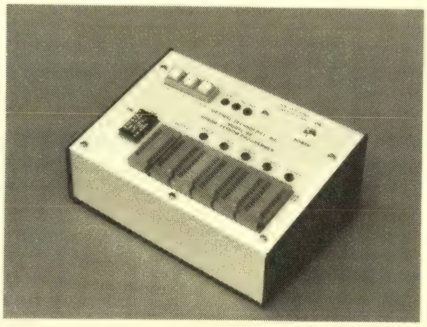

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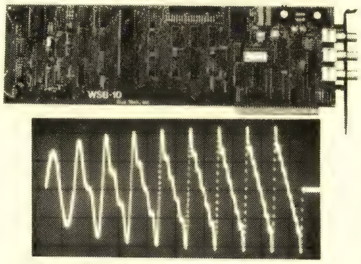

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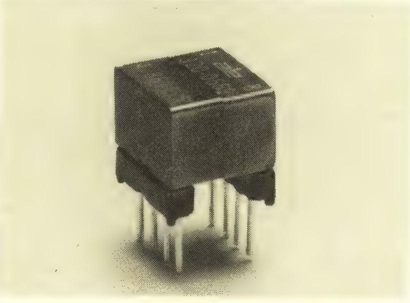

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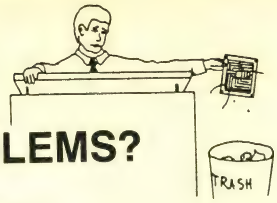

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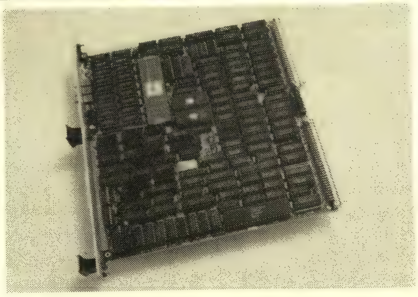

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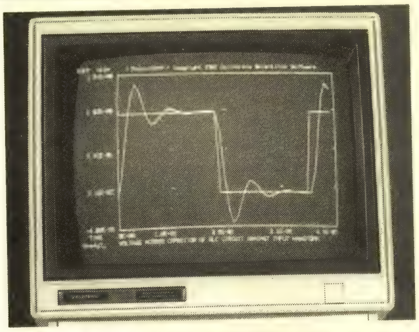

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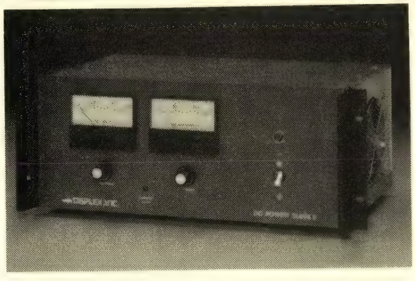

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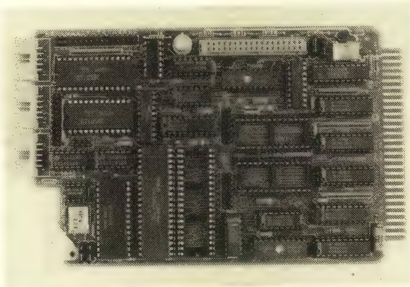

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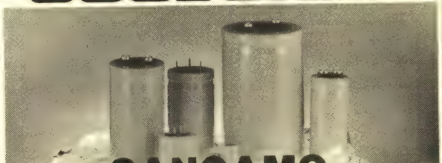

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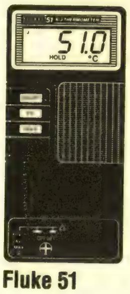

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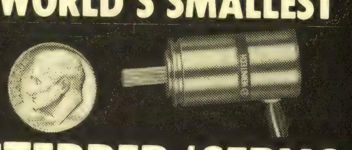

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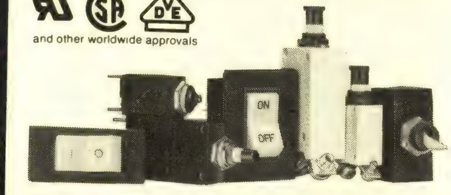

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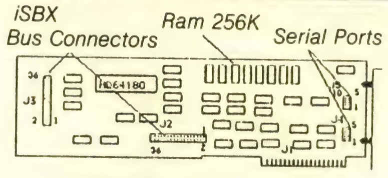

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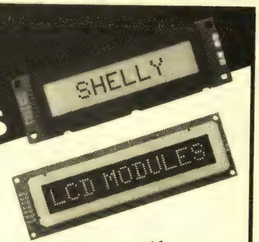

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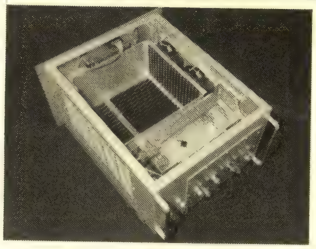

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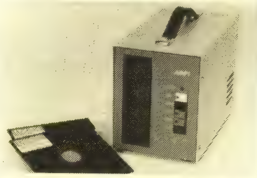

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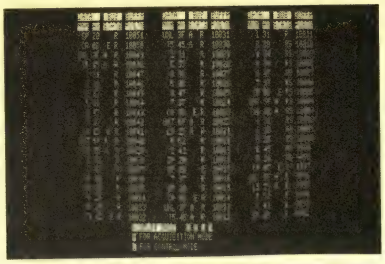

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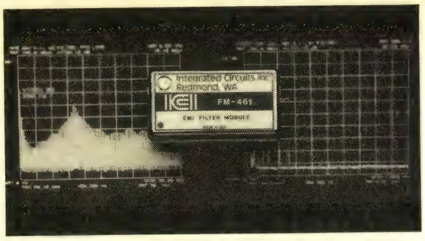

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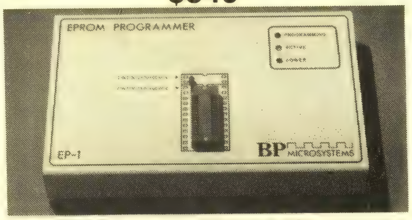

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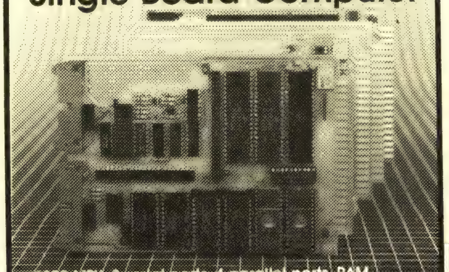

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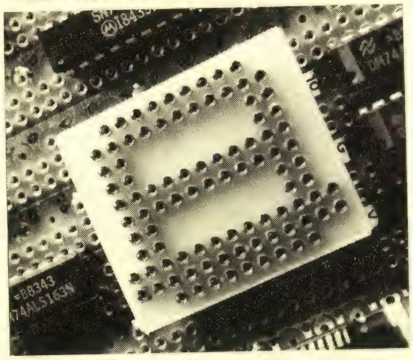

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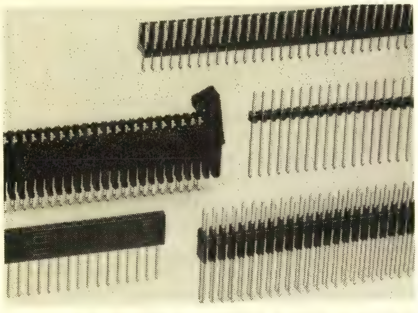

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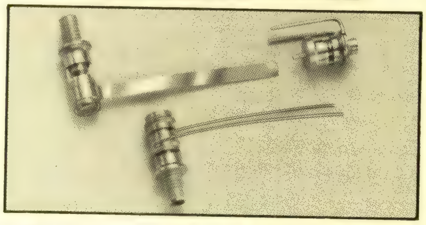

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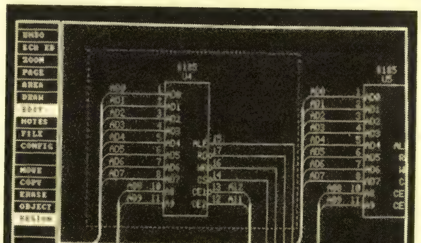

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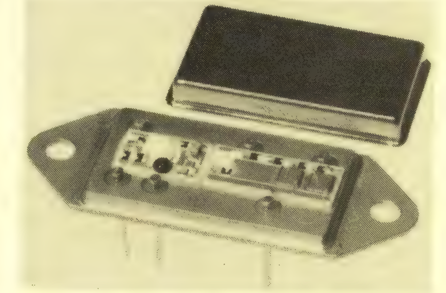

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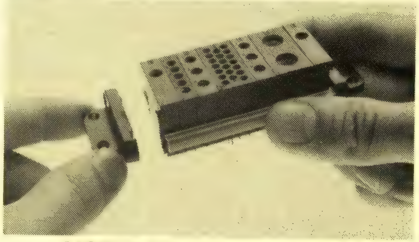

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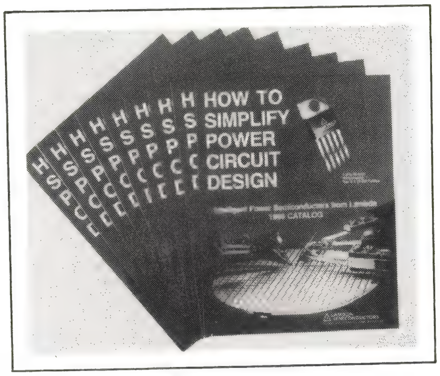
CIRCLE NO 159

Supplement to component catalog

This 1986 12-pg supplement to *Catalog #888* features more than 200 additions to the manufacturer's line of components and hardware. The brochure contains information on such products as test leads (right-angle, shrouded, and banana plugs); test-lead accessories (hooks, alligator clips, spade lugs); jumper cables and patch cords; battery holders and clips; and grommets, bushings, and washers. In addition to an alphabetical table of contents, the pamphlet includes an index that lists the catalog number for each product described.

Keystone Electronics Corp, 49 Bleecker St, New York, NY 10012.

Circle No 351



Catalog details semiconductors

How to Simplify Power Circuit Design is a 20-pg short-form directory to 160 of the company's standard power semiconductors, including PWM controllers, switching regulators, power drivers, power Darlingtons, half-bridge dual rectifiers, 0V protectors, and linear regulators. The catalog also lists 10 new products, including the LSH 6300 dc/dc microconverters and the LAS 8091P and 8071P 4-channel output drivers. It contains detailed specification charts, diagrams, and distribution pricing information on all semiconductors covered.

Lambda Semiconductors, 121 International Dr, Corpus Christi, TX 78410.

Circle No 352

Publication describes power tubes and cavities

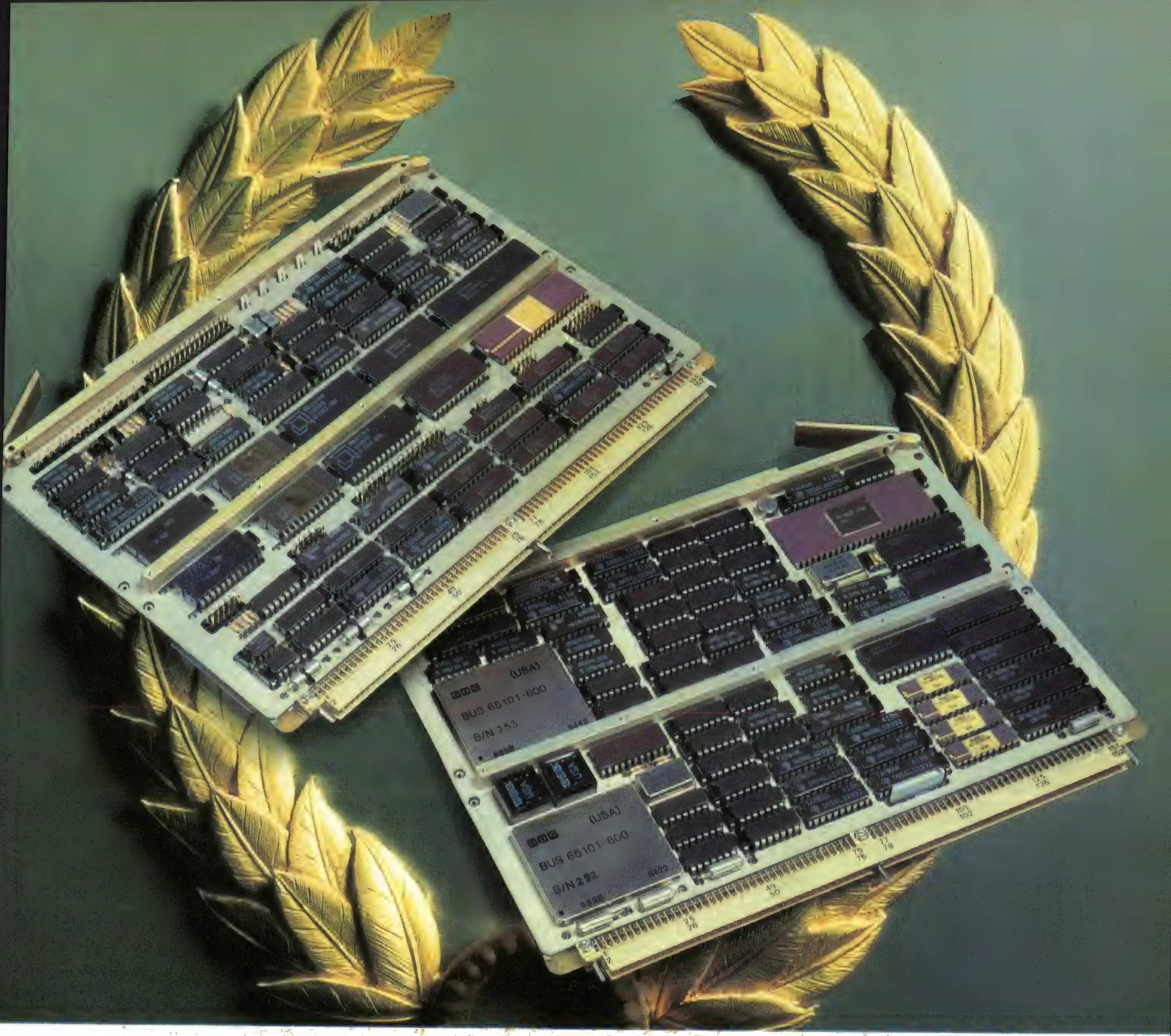
Power Tubes, a 52-pg product guide, gives technical data on the manufacturer's line of tubes and associated components. The guide features separate sections for broadcast, communications, and special-purpose types as well as a section on tube characteristics. The broadcast section includes a quick-reference guide for selecting tubes and cavities for various AM, FM, and TV applications. Other selection guides encompass other types of tubes.

RCA, New Products Div, Tube Operations Marketing, New Holland Ave, Lancaster, PA 17604.

Circle No 353

Guide to Unix and C

A pocket reference for Unix and C, the *Text Processing Reference*, is a guide to all Unix word-processing tools and includes data on mm macros and the tbl, eqn, nroff, and troff commands. The 32-pg booklet costs $6. The company also offers several other pocket guides. Each *Unix Command Summary* (for System V, III, Xenix 5, and BSD 4.2) contains alphabetical condensations of the commands accessible by the Unix user. Each booklet includes editor and shell commands and costs $6. The *VI Reference* summarizes



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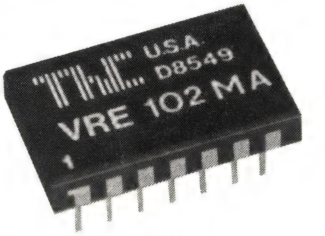

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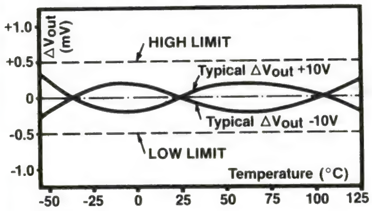

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CIRCLE NO 166

Berkeley's visual editor and costs $3. The *C Library Reference for Standard System V* details the library functions available to the C programmer using Unix; it costs $6.

Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155.

INQUIRE DIRECT

Directory of companies involved in AI

The 1986 edition of *The Artificial Intelligence Directory* covers more than 300 companies involved in AI, expert systems, voice-recognition systems, artificial vision, natural language, symbolic computing, and AI programming languages. The softbound, 8½×11-in. book includes company name, address, and telephone number; names of individual contacts; facts on corporate activity and products; alphabetical listing of company profiles; and a master telephone directory. $49.95 ($64.95 international).

DM Data Inc, Publications Dept, 6900 E Camelback Rd, Suite 1000, Scottsdale, AZ 85251.

INQUIRE DIRECT

Data sheet describes 5-MHz V/F converters

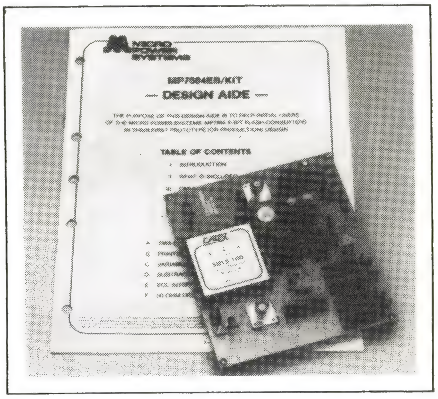
This revised data sheet covers the 3805 and the 3825 Series of 5-MHz V/F converters. It describes the six models of single-ended and differential-input V/F converters, including features and specifications as well as general-usage and specific-application information.

Dymec Inc, 8 Lowell Ave, Winchester, MA 01890.

Circle No 356

Guide aids in designing flash converter

The *MP768EB/Kit Design Aide* assists engineers in the design, development, and test of a prototype 8-bit flash-converter system based on the MP7684. The kit contains the necessary data and pc-board layouts for building an evaluation board, including product description, schematic, assembly drawing, applications section, interfaces section, and parts list.



Micro Power Systems Inc, 3100 Alfred St, Santa Clara, CA 95054.

Circle No 357

Disk explains pc-board CAD

This combination demonstration disk/synchronized audio cassette allows you to preview the vendor's Quik Circuit pc-board layout system before deciding whether you should buy it. The program runs for 35 minutes, but you can stop it at any time to put the software through its paces on your own. The disk—as well as the actual pc-board layout software—runs on a Macintosh (with at least 128k bytes), XL, Lisa (with Macworks), or Macintosh Plus. $15; pc-board layout software, $695.

Bishop Graphics CAD Systems Corp, 5388 Sterling Center Dr, Westlake Village, CA 91359.

INQUIRE DIRECT

Guide helps in selecting active filters

This design and selection guide covers lowpass, highpass, and bandpass/reject filters and high-purity sine-wave oscillators available in fixed-frequency, resistive-tunable, and digitally programmable models. It also details filters for telecommunications and antialiasing applications. The 245-pg book contains a

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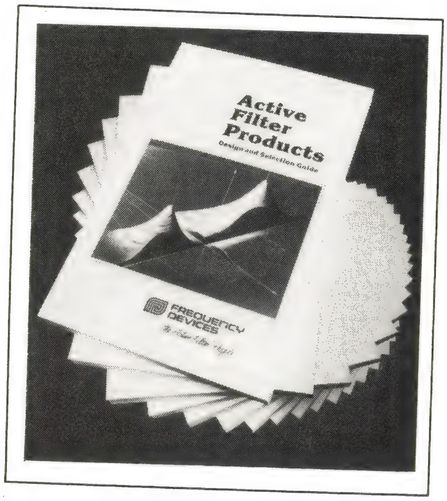


glossary of technical terms, complete specifications for 56 product families, and a 25-pg tutorial section on active-filter theory, design, and applications.

Frequency Devices Inc, 25 Locust St, Haverhill, MA 01830.

Circle No 359

Brochure touches on motion controllers

This short-form brochure briefly describes the company's motion-control products. These include the dc Servodisc armature motors, ranging from less than 1/25 to 10 hp, the dc Servodisc gearmotors, PWM servo amplifiers, and the Synchrostep step motors and chopper drives. In addition, it highlights a series of optical encoders.

PMI Motion Technologies, 49 Mall Dr, Commack, NY 11725.

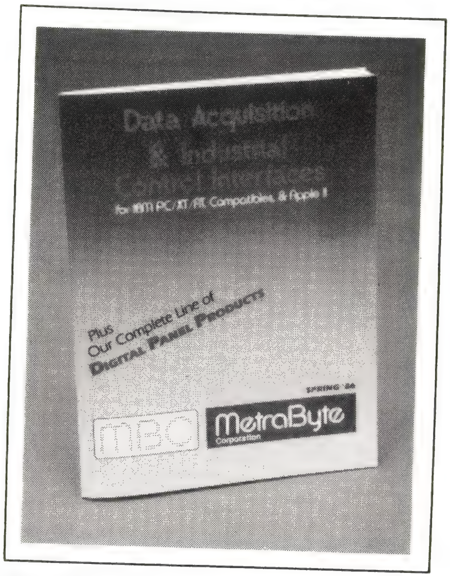
Circle No 360

Brochure features electromagnetic delay lines

Catalog 27D presents this company's line of electromagnetic delay lines and introduces three newly expanded series: video and pulse delay lines, variable delay lines for radio-paging systems, and T0-5-style lumped-constant delay lines. The 24-pg catalog also covers VES Series fixed delay lines; HF, HR, and VHR delay lines; and a group of fixed attentuators. Finally, it highlights its Spiradel family of high-ratio, distributed delay lines.

Allen Avionics Inc, 224 E 2nd St, Mineola, NY 11501.

Circle No 361


Data Acquisition & Industrial Control Interfaces
for IBM PC/XT/AT Compatibles & Apple II
Plus Our Complete Line of Digital Panel Products
Spring 86
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MetraByte Corporation

Handbook catalogs interfaces for PCs

This handbook describes the company's plug-in boards suitable for data-acquisition and industrial-control interfaces for personal computers as well as communications interfaces for IBM PCs, PC/XTs, PC/ATs, and compatibles. It also features new digital panel meters and printers. The 130-pg book provides technical specifications and pricing information, along with application and product-configuration guides.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780.

Circle No 362

High resolution, rugged CRT's for avionics ... a brighter idea from AEG!

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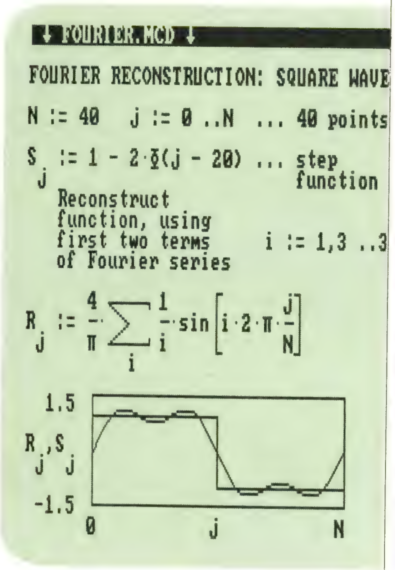
CIRCLE NO 172

MathCAD

The Engineer's Scratch Pad



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N := 40   j := 0 ..N   ... 40 points
S  := 1 - 2·Φ(j - 20) ... step
 j                         function
   Reconstruct
   function, using
   first two terms      i := 1,3 ..3
   of Fourier series
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BUSINESS/CORPORATE STAFF

F Warren Dickson
Vice President/Publisher
Newton, MA 02158
(617) 964-3030
Telex 940573
Diann Siegel, Assistant

Peter D Coley
Associate Publisher/
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Stacey Vorias, Assistant

NEW ENGLAND
Bob Sommer, Regional Manager
275 Washington St
Newton, MA 02158
(617) 964-3030

STAMFORD 06904
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8 Stamford Forum, Box 10277
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103 Eisenhower Parkway
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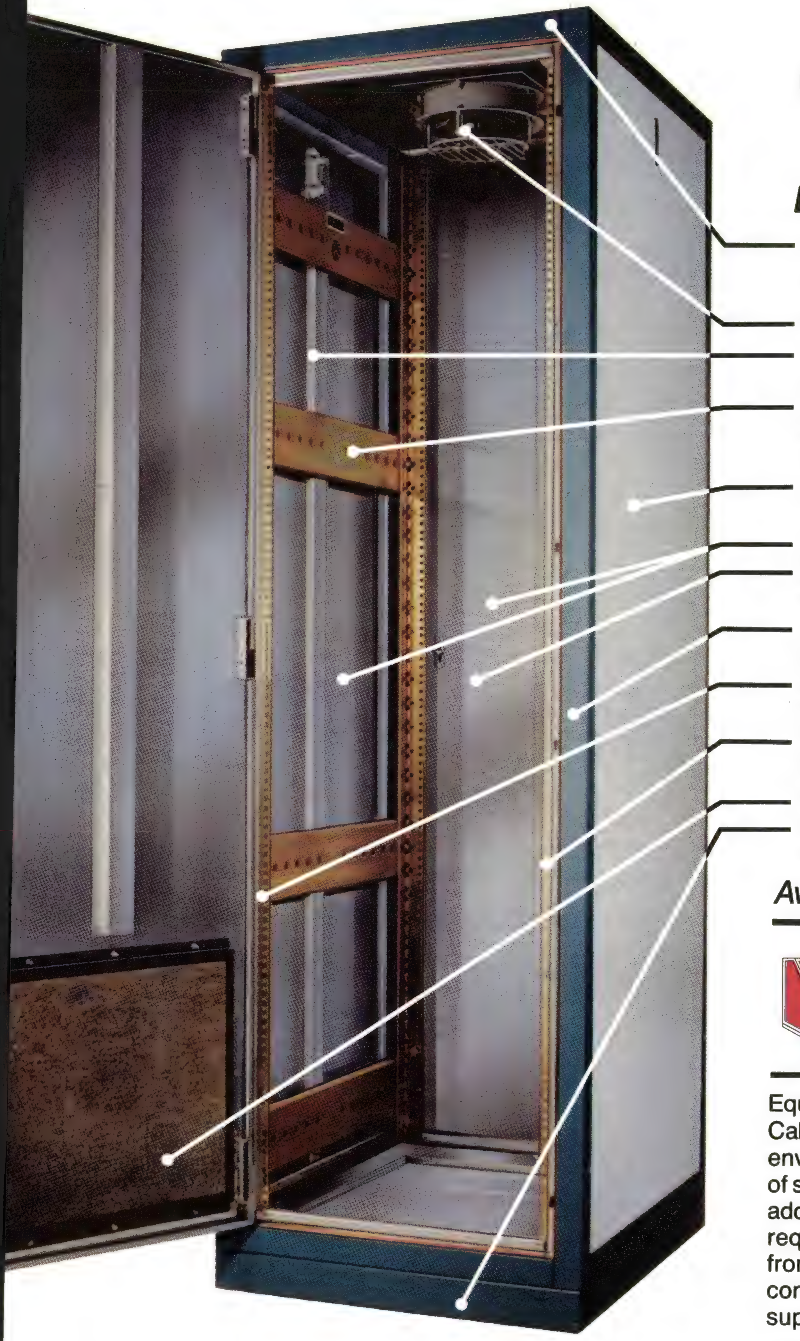

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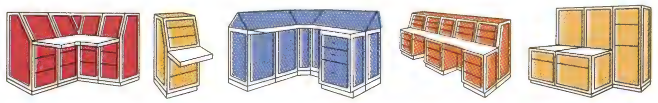

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CIRCLE NO 164

MARKET FORECASTS

Opto-Electronic Market Opportunities (#672). 212 pgs; $1850; International Resource Development Inc, 6 Prowitt St, Norwalk, CT 06855.

Encompassing the entire opto-electronic market including military and civilian, consumer and industrial, and component and system categories, this report analyzes the current market size, market growth, competitive situation, and state of the art in each segment.

The Market for Switches in the Electronics Industry: A Strategic Analysis. 200 pgs; $3250; Venture Development Corp, Box 9000, Natick, MA 01760.

This report discusses the major factors influencing the development of this market including foreign competition, substitute products and alternative technologies, and channels of distribution. Included are dollar and unit forecasts by product category as well as projections by business segment. Manufacturers' market shares for total switch production and for each specific product category are listed. Shipment data by product category is included, along with profiles of the 28 largest vendors.

Fiber Optics: Optical Fiber Communications Link Design Performance Standards for Long Haul Telecommunications Applications. Vol #9; $100; Information Gatekeepers Inc, 214 Harvard Ave, Boston, MA 02134.

An addition to the "IGI Users Manual Series for Fiber Optics," this report follows an engineering approach to the design of optical fiber communication links to meet mandated specifications for performance and interoperation. It expands upon technical guidance originally developed for MIL-STD-188111 Subsystem and Design and Engineering Standards for Common Long Haul and Tactical Fiber Optic Communications.

Customizing VLSI Integrated Circuits Update—A Users Guide to the IC Design Center and ASICs. 275 pgs; $985; Electronic Trend Publications, 10080 N Wolfe Rd, Cupertino, CA 95014.

This report examines the converging market and technology trends influencing the electronic systems OEM. Its goal is to assist the OEM in utilizing the IC design expertise at more than 150 North American design centers. The report describes the custom and semicustom options available to the ASIC user and how these chips can be tailored to meet specific price and performance criteria. Included is a full comparative analysis between gate arrays, standard cells, electrically programmable logic, and full custom ICs. The report profiles major suppliers of silicon services to the OEM, including IC design houses, mask makers, packaging houses, foundries, test and assembly houses, and semiconductor manufacturers.

The Pressure Transducer and Transmitter Industry: A Strategic Analysis, 3rd ed. 237 pgs; $3250; Venture Development Corp, Box 9000, Natick, MA 01760.

Based on data collected through surveys of manufacturers and users, this report provides 5-year forecasts segmented by product technology and industry segment. It claims that the market for pressure transducer and transmitter will reach almost $1.2 billion by 1990. It gives vendor market shares and strategic recommendations and profiles more than 90 industry participants.

Test Equipment Use by Computer Equipment Manufacturers. $895; Market Intelligence Research Co, 4000 Middlefield Rd, Palo Alto, CA 94303.

This report gives the results of a survey focusing on questions such as what test equipment is used by production plants in the computer industry, what current test needs are, what test needs will be in the future, and how the future of the electronics industry impacts current and projected demand. Sixty-six plants are surveyed and categorized according to size, primary product, volume of boards tested per week, and the type of CPU used in their products. Information is presented in both text and tabular form. Also included are discussions on current and future test needs.

1986 Hardware Trends in Engineering Computer Graphics. 16 pgs; $25; CAD/CAM Technologies Inc, Box 62, Minneapolis, MN 55415.

This report discusses the role of the mainframe, mini, and personal computers in establishing a system network which allows replication of human design and engineering processes. The latest developments in computer processors, display devices, cursor controls, output devices, and data storage technology are included.

The Impact of the 32-Bit Microprocessor on the Computer Systems Market. 200 pgs; $795; Electronic Trend Publications, 10080 N Wolfe Rd, Cupertino, CA 95014.

This report examines the issues surrounding the growth in microprocessor capabilities and the devices' impact on manufacturers and component suppliers. It covers key technological issues such as on-chip cache, virtual memory management, operating system support, language support, and peripheral device support chips that will determine success or failure in the marketplace of the various 32-bit competitors. Also included is a 1984-1990 forecast of the microprocessor market growth and market shares.

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NEW BOOKS

Foiling the System Breakers: Computer Security and Access Control, by Jerome Lobel. 292 pgs; $34.95; McGraw-Hill Book Co, New York, NY, 1986.

This book presents information on planning, organizing, directing, and controlling an information system. The author suggests specific standards for handling confidential, proprietary, or classfied data. Other topics discussed include identifying potential weaknesses in data-communications networks, ensuring that security controls are not circumvented, creating a system for user clearance and data classification, and balancing operations and productivity with security and control. Numerous examples, charts, and graphs help to clarify and amplify key principles and techniques.

The author also covers trends in computer fraud and industrial espionage; software piracy; the automation of information security policies, passwords, and personal identification devices; access control software; and database and network security. Other subjects include closed- and limited-access networks, office-automation systems, personal-computer protection, and security monitoring and feedback.

Analog Printed Circuit Board Design and Drafting, by Darryl Lindsey. 430 pgs; $149.95; Bishop Graphics Inc, Westlake Village, CA, 1986.

This combination text and companion kit of professional design and drafting aids can teach you the intricacies of analog printed-circuit design and drafting by allowing you to perform actual pc-board design and artworks. Numerous "how to" exercises guide you through pc-board layouts. The author gives thorough explanations of schematic diagrams, an in-depth description of components and pc-board packaging, and an analysis of pc-board design considerations.

An Introduction to Program Verification, by Ali Mili. 312 pgs; $37.95; Van Nostrand Reinhold, New York, NY, 1985.

The book provides you with eight program-verification techniques and gives you step-by-step guidance for understanding and using these techniques. Topics include set theory, relations, functions, and lists; fundamentals of mathematical inductions in strictly ordered and well-founded sets; proof of recursive functions; and program design by predicate, functional, and relational decomposition.

Personal Engineering Resource Directory, compiled by Lotus, Engineering & Scientific Products Div; Lotus Development Corp, Cambridge, MA, 1986.

This directory lists microcomputer products and services specifically designed for engineers and scientists. The products are listed alphabetically by application. Each listing contains a brief description of the product, its compatibility with Lotus products, hardware and software requirements, price, and the name and address of the vendor. Also included is a list of reference materials such as books, articles, and training resources, as well as indices listing the products by name and vendor.

Multidimensional Systems: Techniques and Applications, edited by Spyros G Tzafestas. 656 pgs; $79.75; Marcel Dekker Inc, New York, NY, 1986.

This book consists of contributions by internationally recognized experts that describe the state of the art of multidimensional system (MDS) techniques and applications. It gives you a broad range of alternative designs and solutions. Some of the topics include 2-dimensional linear-system design methods dealing with digital finite and infinite impulse response filtering or local-space processing; recent techniques and results on stability analysis of 2-dimensional systems with extensions to multidimensional systems; degradation in 2-dimensional digital-filter performance due to finite-word-length effects; computer-aided design of 2-dimensional digital filters; and digital tomographic filtering used in radiographs. Numerous graphs, drawings, and photographs are also included.

Power Integrated Circuits, Physics, Design, and Applications, edited by Paolo Antognetti. 544 pgs; $42.50; McGraw-Hill Book Co, New York, NY, 1986.

This comprehensive reference contains information by 16 internationally recognized authorities covering all the aspects of power-integrated circuits (PICs), including power MOS devices. Some of the topics covered include reliability problems such as electromigration, parasitics MOS, and thermomechanical effects; solutions to many often overlooked packaging problems; electrical and thermal limitations; and a way to protect PICs against stresses caused by the use of high power. Numerous graphs, tables, and plots help clarify the design, development, and implementation of current PICs.

Working Safely With Robots, edited by Peter Strubhar. 260 pgs; $35; Society of Manufacturing Engineers, Dearborn, MI, 1986.

This book consists of 30 current articles providing information on how to minimize the risk of injury by an industrial robot. The book tells you how to implement the robotic safeguards that will be effective in your own operations. Specific chapters cover philosophies, human factors, installation, maintenance and construction, safety training, and standards for working safely with robots.

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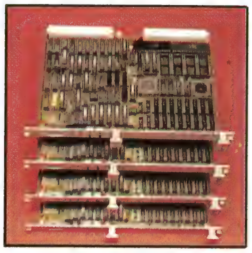
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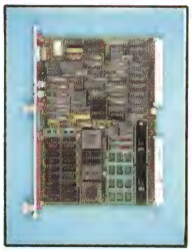
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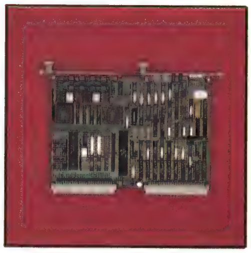
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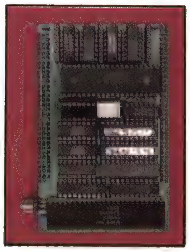
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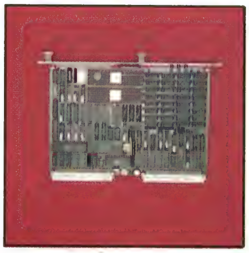
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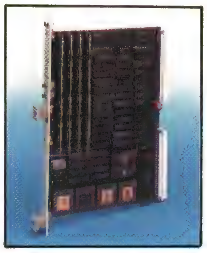
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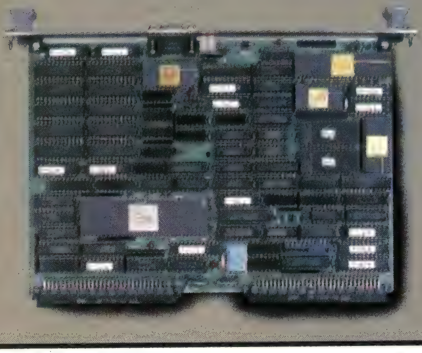

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CIRCLE NO 167

PROFESSIONAL ISSUES

Consulting engineers pay a high price while fighting for liability law reform

Deborah Asbrand, *Staff Editor*

Engineering organizations have joined ranks with architects, doctors, accountants, and child-care workers to support changes in liability laws that would protect their members in private practice from rising insurance premiums and the threat of lawsuits. And it is consulting engineers, as opposed to engineers who work for large companies, who must individually shoulder the financial onus of liability insurance. The help they need could come from a variety of organizations that are pushing to reform state and federal liability laws.

Increasingly large damage awards in suits that involve consulting engineers have led insurance companies to raise their premiums and their deductibles. In 1985 alone, premiums for the liability insurance endorsed by the National Society of Professional Engineers rose 35%.

Civil and structural engineering consultants are feeling the most intense pressure. Statistics from the American Consulting Engineers Council (ACEC), a Washington, DC, organization, reveal that in 1981, independent consulting firms in these two disciplines spent 3.31% of their billings on liability insurance; in 1985, that figure rose to 4.5%. Moreover, for every 100 civil and structural engineering firms in 1985, 109 suits were filed.

Electrical engineering consultants are also open to damage suits and the resulting insurance pinch. “If a worker is injured while working on an electrical system, he can sue the engineer who designed the system for not ensuring his safety,” says Steve Church, ACEC assistant director of information and communications. In 1985, the ACEC found, 20% of the independent mechanical or electrical engineering consulting companies who belong to the trade group faced law suits.

Like structural engineers, mechanical and electrical engineering consultants have seen their liability insurance costs rise. In 1981, these engineering consultants spent 2.24% of their billings on liability insurance; in 1985, they spent 2.52%. Although insurance costs for mechanical and electrical engineering consultants haven’t risen as steeply as those for structural engineers, the increase in cost plus the expensive complications of litigation have caused some alarm among the insurance companies: As of June 1, the IEEE’s Professional Liability Plan was canceled by its insurance company. Just over 1000 IEEE members belonged to the plan.

Other insurance companies have also stopped offering liability insurance for architects and engineers as a result of mounting damage awards. Of the 10 companies that once underwrote liability insurance for architectural and engineering consultants, only four companies continue to provide such insurance, says Church.

To gather support for liability reforms, ACEC representatives spearheaded the formation of the American Tort Reform Association (ATRA). More than 300 organizations have joined ATRA since its formation in January, including the American Association of Engineering Societies and the National Society of Professional Engineers (NSPE). In February, leaders of 150 of ATRA’s member organizations traveled to Washington, DC, to meet with Attorney General Edwin Meese. Their strategy worked: The Reagan administration took up their cause and backed legislation aimed at reducing professional liability.

Michael McLaughlin

Among the liability legislation filed in the Senate was a bill by Senator Robert Kasten (R-WI) that would require product liability to be based on a specific and substantiated fault attributable to an individual. It also voids the concept of "joint and several" liability, which allows a defendant found guilty of 1% of the damages to be held accountable for the entire damage award if it's established that the other defendants cannot pay. In addition, Kasten's bill would place a $100,000 cap on awards for pain and suffering and implement a sliding scale for lawyer's contingency fees. This latter provision states that a lawyer obtains a fixed percentage of any damage award in direct proportion to increases in the gross amount. ACEC's Church considers the cap on pain-and-suffering awards to be crucial: "The killers in liability cases are the non-economic claims," he says. (Non-economic claims are those such as pain-and-suffering claims that are not directly based on specific financial loss, such as loss of property or income.)

Despite the legislation's White House backing, its supporters are not optimistic about its passage. "I don't know if anyone holds out much hope for [the bills]," says ACEC's Church. "People on Capitol Hill tend to focus on issues, and right now their interests are tax reform and the Superfund [for toxic wastes]." Milton Lunch, NSPE general counsel, agrees with Church's assessment of the fate of proposed federal legislation. "Nothing's going to happen with product liability in Congress this year, and that's almost a sure bet," Lunch says.

> *"The killers in liability cases are the non-economic claims," says Steve Church.*

Because tort law is governed by the states, Lunch sees local legislatures as the seats of action for liability reform. Bills were filed in more than 20 states this year, and some progress has been made. In June, California voters gave liability reformers a victory when they limited the legal rule of joint and several liability to compensation for financial loss. In addition, under the new rule, defendants will be required to pay only for the pain and suffering that they have personally caused. Maryland, too, has legislated limits on awards for non-economic damages. Utah and Washington have already joined the fight by passing laws that restrict joint and several liability. **EDN**

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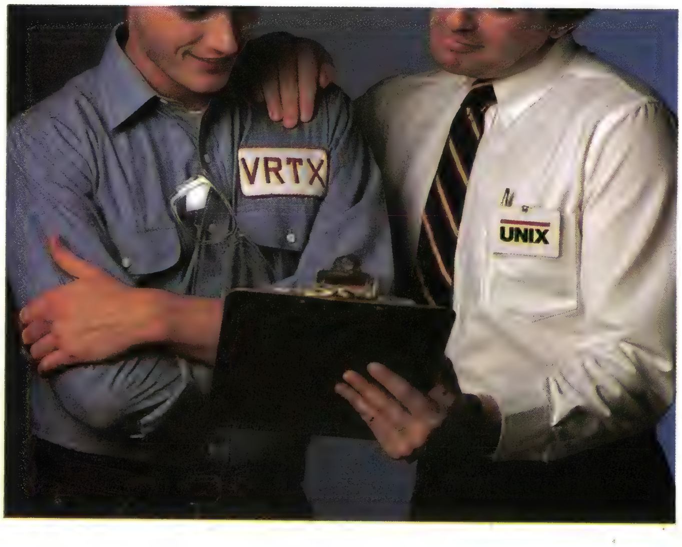

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CIRCLE NO 170

When Stanford recruits for its MSEE program, the name of the game is personal attention

Deborah Asbrand, *Staff Editor*

Michael McLaughlin

Times have certainly changed for well-qualified engineering students aspiring to graduate programs. Ten years ago, even the best applicants to these programs could only hope that their transcripts and test scores would suffice to impress admissions officers. Now, as competition for the top students builds among universities, it's the schools that are out to impress the students. Nowhere is this change more evident than at Stanford University, where top applicants can now expect phone calls from department representatives thanking them for their interest in the school and encouraging them to call collect if they have further questions. To reinforce the recruiting effort, individual faculty members also telephone prospective students with whom they share technical interests.

Stanford's admissions process wasn't always so aggressive. In the past, reviewers scrutinized the approximately 300 MSEE applications that the school receives each year and identified the top 50 students. Of that group, the top 20 students received fellowship offers for as much as $20,000. However Stanford's admissions office, responsible for administering the grants but already bogged down in the general crush of acceptances for the following September, often notified recipients of their awards later than did other schools. Furthermore, no follow-up calls were ever placed. And worse yet, any grants that were turned down by the first-round candidates remained unused.

Stanford's haphazard admissions procedure cost the school in its ability to attract the most sought-after applicants, who usually receive offers of financial aid from several schools. In many cases, students had already elected to attend other schools by the time Stanford's fellowship offer reached them. Some years, as many as 10 of the fellowships were turned down and went unused. As a result, Stanford's success rate in courting its top applicants was 60%—a figure university officials considered too low. And the school's record for attracting the remaining top students to whom fellowships were not extended was even lower, just 35%.

To improve its appeal to students, the university hired a part-time recruiter for its MSEE program. Since Rick Reis, assistant director of Stanford's Center for Integrated Systems, took on the job four years ago, the university has boosted its share of the pool of top MSEE applicants to 80%. In addition to telephoning applicants and personally acknowledging applications, Reis's strategy includes escorting visiting applicants around the campus. He has also transferred responsibility for offering fellowships—and following up on those offers—to the electrical engineering department, so that Reis himself now dispenses all 20 grants each year.

Although Stanford's recruiting policies have been highly successful, other top engineering schools take a more understated approach to recruitment. "We write letters to the top students guaranteeing them [financial] support," says Joel Moses, head of MIT's Department of Electrical Engineering and Computer Science. "And there may also be phone calls from faculty members to some of the applicants, but I don't see any major campaign going on." **EDN**

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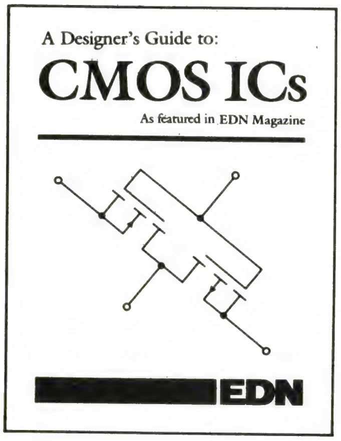

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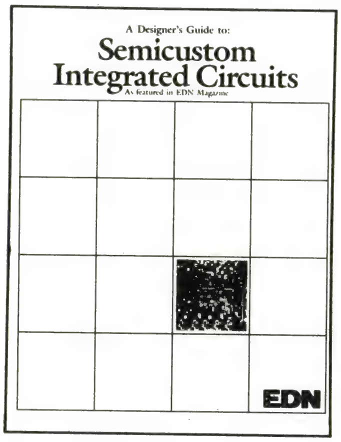

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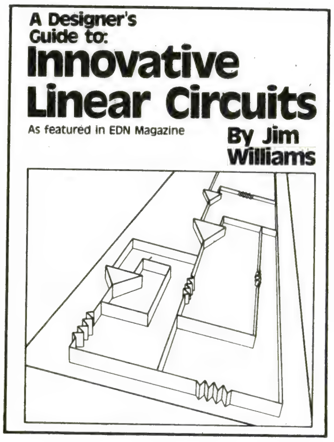

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Oct. 16	Sept. 25	Digital Signal Processing; Personal Computers; ICs; Test & Measurement Instruments; Display Technology	
Oct. 30	Oct. 8	Batteries; Converters; Wescon '86 Product Preview; European Electronics; Computer Boards	
Nov. 13	Oct. 23	Wescon '86 Show Issue; Op Amps; CAE; Semicustom ICs (CAE- related*); Artificial Intelligence (CAE-related*)	Closing: 11/3 Mailing: 11/25
Nov. 27	Nov. 6	Microprocessor Technology Report & Directory; CAE; Passive Components	
Dec. 11	Nov. 18	Product Showcase—Volume I; ICs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products	
Dec. 25	Dec. 4	Product Showcase—Volume II; Computers & Peripherals; Components; Test & Measurement Instruments; International Products; Literature on ICs & Semiconductors, Hardware & Interconnection Devices, Power Supplies/Sources, Software	

Call today for information.

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National: Roberta Renard (201) 228-8602

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Requires a BS or BA in an engineering discipline, MS or MBA preferred, and 10 years of DoD configuration management experience which includes experience chairing a configuration control board. Experience with configuration identification, configuration status accounting, configuration audits and reviews. Working knowledge of DoD STD 480, 481, MIL STD 1521 is required.

Reliability Engineering Manager

Requires a Bachelor's degree in Engineering and 8+ years experience in a Department of Defense, Reliability/Maintainability Supervisory environment. MBA or MS in engineering desirable. Extensive knowledge of MIL-STD 785 and MIL-STD 470 is required.

Focus on the future with Fairchild Weston. We offer an excellent salary, a full range of company benefits, and a choice suburban Long Island location. For details, send your resume and salary history, to: R. Magnus, Professional Staffing, Dept. 82X, Fairchild Weston Systems, Inc., 300 Robbins Lane, Syosset, NY 11791.

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Ability to assume project responsibility and technical supervision. Requires a minimum BSEE with 5-10 years experience in RF/MW circuit design and analysis. Some background in solid state amplifier design is preferred.

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High performance computer architectures

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If you've got a BS, MS, or PhD and at least two years' experience, particularly in Systems Engineering, Signal/Image Processing, Microwave Design, Digital/Microprocessor Design or Software Development, send your resume, in confidence, to: Jack Howell/Texas Instruments/P.O. Box 405, M.S. 3426/Dept. EDN/Lewisville, Texas 75067.

Better yet, call Mr. Howell at 1-800-527-5864. In Texas, call collect: 214-462-5746.

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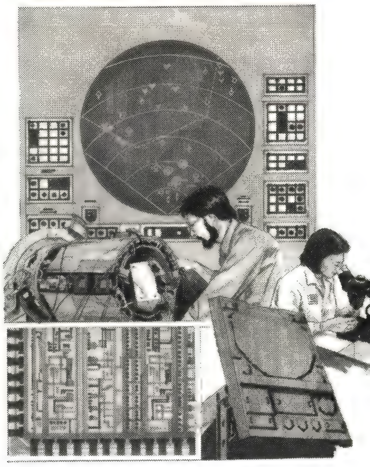

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☐ Requires degree in Mathematics, Computer Science, Engineering or Physics with 1–10 years applicable work experience

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☐ Plan and conduct studies to establish weapon systems requirements relative to sensors, engagement operations, employment/deployment as well as develop and evaluate alternative system concepts for air-to-air, air-to-ground, and surface to air missile systems
☐ Will also predict system performance for trade-off and cost/effective analysis
☐ Requires appropriate technical degree and 3+ years related experience

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☐ Establish system requirements for operation with TADIL-B, and JTIDS communications systems, determine hardware requirements and plan and analyze test
☐ BS plus 1–10 years experience required

Guidance and Control

☐ Utilize modern estimation and control techniques to design guidance logic and flight control systems for advanced missile concepts including defining subsystem requirements for seeker stabilization, inertial sensors, actuators and algorithms to meet system goals
☐ Requires BS/MS with experience in aerospace vehicle control systems

Radar/Surveillance Analysis

☐ Develop and evaluate logic for radar surveillance operations using analysis and simulation techniques
☐ Requires understanding for signal processing techniques (MIT, pulse doppler, etc.)
☐ BS in Engineering or Physics with 2–10 years experience required

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☐ Participate in the development of large scale simulations of missile systems
☐ Will design models for implementation in six degree of freedom digital simulations and hardware in-the-loop test facilities
☐ BS in Engineering, Computer Science, Math, or Applied Science required

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☐ Analyze propulsion system performance and specify requirements for preliminary design studies, monitor development and qualification of propulsion systems from vendors, and provide guidance for identifying and developing future propulsion systems for advanced vehicle designs
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Ordnance

☐ Perform analyses and simulation of missile ordnance and fusing functions; develop vulnerability models; and determine effectiveness against targets and optimize armament performance
☐ Requires BS/MS and 5+ years related experience.

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☐ Generate performance requirements, implement trade-offs, and engage in proposal preparation

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☐ Task range from analog video circuits to microprocessor hardware/software
☐ Involvement with CAD/CAT

Antenna Design and Development

☐ Design and development of wideband airborne antenna systems
☐ Antenna types include phased array and lens
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Missile Guidance Circuits

☐ Development of integrated circuit computer models as used in analog low frequency devices
☐ Familiarity with analog/digital circuits as used by servo control and low frequency electronics

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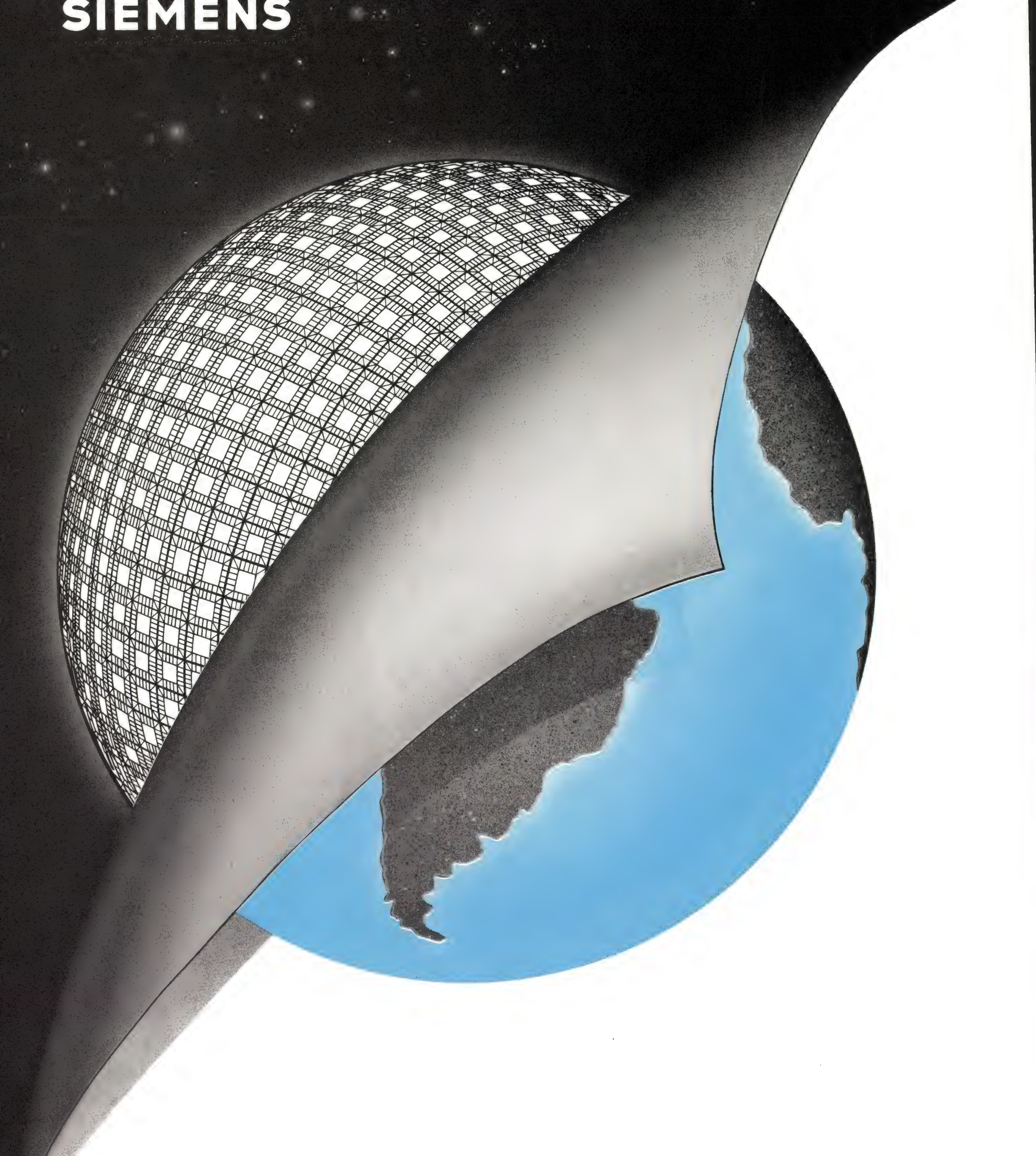

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Requires a BSEE or equivalent with 3 to 5 years' marketing experience and a strong background in either optoelectronics, semiconductors, or the military components marketplace.

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Requires a BSEE (MSEE preferred) and 5+ years' systems experience. Proficiency in power transistor circuit design/troubleshooting, MOSFET circuits and process technology necessary.

PACKAGING ENGINEERS

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Responsible for marketing activities of multinational strategic accounts throughout the United States, you will negotiate multinational contracts, identify new business opportunities for these accounts and develop close working relationships with strategic accounts to define future product generations. Requirements include a technical degree and related experience.

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- **Laboratory Test Facilities**
- **Maintainability**
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- **Instrumentation**
- **Controls and Accessories**

Manufacturing

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- **Machining Design**
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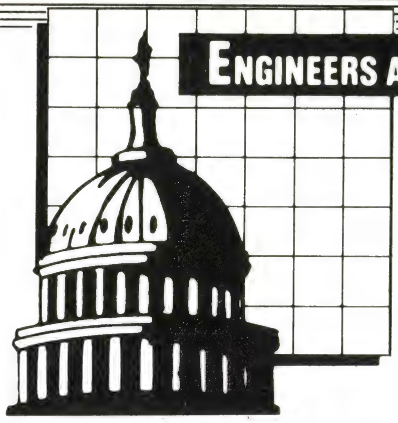

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- EW/ESM/ECM systems
- AI/Expert systems
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- Receiving and Processing subsystems
- Real-time processing
- Signal analysis
- RF tracking systems
- Over-the-horizon radar

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- Digital signal processing
- Microprocessor hardware/software
- Communications signal processing

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  - —Relational DBMS
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  - —Microprocessor applications (Motorola 68020)
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  Interdisciplinary software/firmware/hardware teams build systems from high-level design through final test and integration using skills in:
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  - —Real-time analysis and control
  - —Test-bed development and analysis
  - —Mapping and graphics displays
  - —Man-machine interfacing
  - —Concurrent processing
  - —Software architecture design
  - —Data base design and applications
  - —AI/Expert systems

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CONTROL ANALYST — Will design robust and adaptive controls for multi-variable systems. Requires knowledge of aerodynamics and flight control principles using classic and modern techniques, as well as technologies which can reconfigure in case of failures or damages.

SOFTWARE PROJECT ENGINEERS — Development of flight software for advanced guidance and control systems for aircraft utilizing modular and structured programming techniques. Involves algorithms and development of real-time microprocessor programs in both Assembly and high order language with subsequent integration with hardware. Familiarity with military digital systems standards (MIL-STD-1553B and 1750A).

For the above positions, the selected candidates will have a BSEE and a minimum of 5 years relevant experience.

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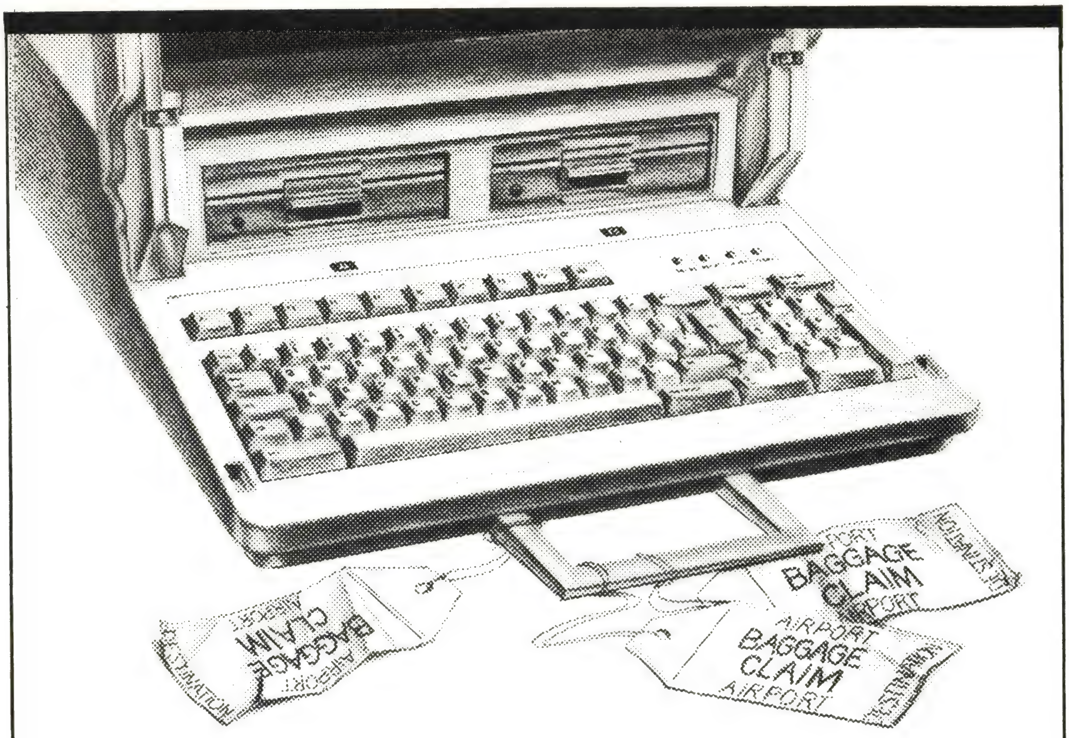

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3 years' ADP experience with at least 1 year's PDP-11, UNIX experience.

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10+ years' digital/analog hardware design experience. MSEE preferred.

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1-5 years' experience testing complex microprocessor-based hardware demultiplexers.

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3-10 years' experience with strong systems background and Digital/RF engineering skills. Must have good marketing/communications skills.

RF TECHNICIANS
2-5 years' experience in testing/repairing complex units such as down converters, RF multi-position non-blocking switches, and PSK modules.

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GALIUM ARSENIDE INTEGRATED CIRCUIT MANAGER

Participate in the design and operation of a prototype GaAs processing laboratory including direction of fabrication and testing of GaAs MMW IC's. Requires PhD or equivalent and a minimum of 5 years experience.

MIC DESIGN SPECIALIST

Develop and "bring on-line" the Pomona Division capability to design and manufacture Microwave Integrated Circuits. Requires BSEE or Physics and minimum 16 years experience including a broad-based microwave circuit design background.

EMC/NUCLEAR HARDENING SPECIALIST

Perform practical techniques for the prevention, detection and correction of circuit upsets caused by electromagnetic and nuclear effects on modern weapon systems utilizing microwave, analog and digital circuits. Must be familiar with DoD standards, their application and the testing methods used to verify compliance. Requires a technical degree and minimum 20 years experience.

IC DESIGN SPECIALIST

Perform advanced design and/or establish and coordinate design projects among groups of 2-10 engineers. Requires 5-10 years experience in digital IC design and a strong background in system design and digital IC design. Experience in analog design with knowledge of CMOS processing highly desirable. Advanced degree preferred.

ACTUATOR DESIGN SPECIALIST

Move projects from board layout through detail design and prototyping into production, along with generating function specifications for fractional horsepower D.C. motors, torque transmission components and feedback instruments. Individual must excel at stress, dynamic, thermal, vibration and tolerance analysis, and possess extensive knowledge of ANSI Y14.5, manufacturing processes, engineering materials and military specifications. BSME with minimum 8 years experience required; MSME preferred. Control system design experience and knowledge of BASIC/FORTRAN programming are desirable. Ability to obtain a security clearance is mandatory.

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General Manager, Radar Systems Division

The professionals of Motorola's ***Government Electronics Group*** *(GEG) have much to say about their company because GEG is a place where innovative ideas are put into action. The result is leadership in the research, development and manufacture of electronic hardware for our country's defense, national security and space programs. If you have the imagination and skill required to extend our technical frontiers, consider the opportunities now available.*

SOFTWARE

Communications Software Engineers

Communications Software Engineers — *Software design and development experience in communications signals collection, processing, and analysis systems for DoD intelligence community customers. Requires experience in state-of-the-art techniques for interfacing array processor microcode to high level microprocessor and minicomputer languages. Requires experience in developing computer software architectures for a wide variety of high speed digital signal processing applications. Prefer BSEE with 5-8 years experience. Contact Jonn Nolitt.*

Software Systems Engineers

Key technical responsibilities in leading a software development effort. Direct experience in design and development of satellite communication systems networks with emphasis on a variety of processor software systems, software programming and communications systems interface. Requires application of Assembly, ADA and other high order languages. Prefer BSEE/BSCS and 5-10 years experience. Contact Jonn Nolitt.

SUPPORT

Strategic Components Engineers

Strategic Components Engineers — *Responsible for strategic planning and delivery of a project's identified electrical and mechanical parts. Requires direct experience in applying MIL-SPEC-E5400, P11268 and MIL-STD-965, 785, 454. Prefer BSEE with 5-7 years related reliability and components analysis experience for a defense contractor or in a semiconductor reliability organization. Contact Jonn Nolitt.*

Reliability Project Engineers

Responsible for managing and conducting electronic reliability and components efforts in engineering and/or production projects. Develops/implements program plans, budgets, schedules, semi-conductor and passive parts selection procedures, documentation approval and problem solving. Involved in design review participation and presentations. BSEE, 7 years related reliability and parts experience desired. Contact Jerry Chadwick.

MARKETING

Proposal Development Manager

Responsible for development and management of a cost effective proposal Preparation Center in Marketing to DoD customers. Requires direct experience in leading Technical Proposal Teams, configuration/acquisition of desk top publishing systems for cost effective proposal writing. Working knowledge of DoD Source Selection, technical writing leadership combined with implementation of proposal strategies will be routinely applied. Candidate will be involved in the budgeting, planning, scheduling and delivering of proposals. Prefer Technical/Advanced Management Degree and a minimum of 10 years experience. Contact Jonn Nolitt.

Join the people of Motorola's ***Government Electronics Group****. The benefits are many, including sunny Arizona — a land as beautiful as it is abundant with recreation and culture.*

For prompt consideration, forward your resume in confidence to the appropriate technical recruiter at Motorola Government Electronics Group, 8201 E. McDowell Rd., Dept. B658, Scottsdale, AZ 85252; (602) 949-3759. An Equal Opportunity/Affirmative Action Employer.
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SENIOR MICROWAVE ENGINEER

Minimum of 10 years' microwave component design and project experience. To be responsible for MIC components and subassemblies which may include switches, attenuators, amplifiers, couplers, limiters, and TTL or ECL drivers.

MIC PROJECT ENGINEER

For MIC switches, attenuators and limiters. Minimum of 5 years' design experience. BSEE degree required.

SALES ENGINEER

This highly motivated individual will be responsible for existing business, as well as promoting new business for a microwave component sales environment. Two years' technical/microwave component experience a must; sales experience a plus.

ELECTRONIC TECHNICIAN

Involves microwave testing of integrated circuit control devices, testing of low-frequency hybrid circuits used to control microwave devices, and repairing and tuning of both types of devices. You should be familiar with microwave tests and test equipment, plus be able to read schematics and repair low-frequency circuits on your own.

MICROWAVE TECHNICIAN

To test and evaluate MIC-type switches, limiters and attenuators to customer and internal specifications. You'll work from drawings, schematics, specifications, flow sheets and schedules. You should have 2-3 years' experience testing microwave components, be familiar with microwave test equipment and measurements, and preferably be familiar with electronic theory.

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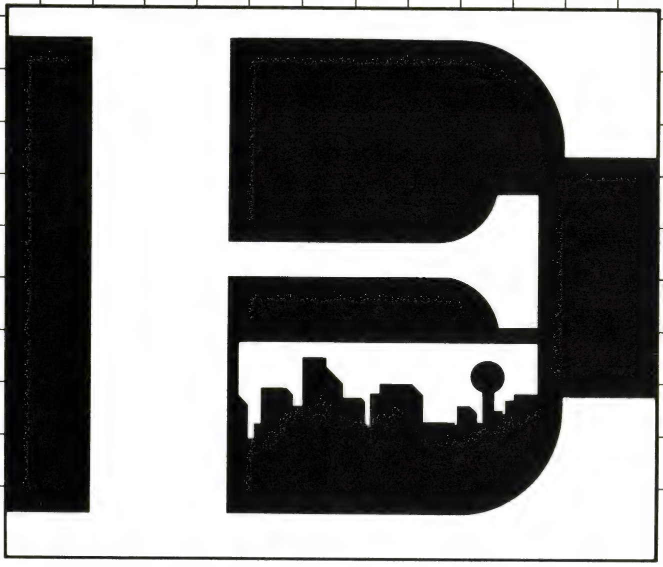

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- Gould Systems Software
- MVS/370/XA or MPX OS

SENIOR HARDWARE SPECIALISTS

Senior Systems Engineers

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- Digital Processing
- Threat Warning
- SIGINT
- ECM
- Electronic Packaging

Senior Design Engineers

- MIC Analog
- Digital
- Synthesizer
- Antenna
- RF/IF Communications
- ECL, TTL Technology

Field Service Engineers

- Receiver Systems Design

SENIOR SOFTWARE SPECIALISTS

Systems and Design Engineers

- Digital Signal Processing
- Digital Image Processing
- Artificial Intelligence
- Operating Systems
- Compression Algorithms
- Communications Protocols
- C^3I
- Hardware
- CICS
- Simulation

SENIOR TECHNICAL SUPPORT SPECIALISTS

Senior Reliability Engineers

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- Part Selection and Substitution
- Reliability Analysis of Digital Reliability Predictions

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SOFTWARE ENGINEERS

BS/MS/PhD EE, CS, or Math with a minimum of 3 years experience in one or more of the following areas:

- Real-time programming
- CMS-2, CMS-2M, Ada®, LISP Languages
- Artificial Intelligence and knowledge based systems
- UYK-20, 7, 43 and 44 and microprocessor based computer languages
- Implementation of state-of-the-art solutions to real-time combat systems
- Engineering problems
- Software testing and quality control
- Information management
- Relational data base design

ELECTRONICS ENGINEERS

- **Digital Design**—High speed militarized local area network (LAN) experience required including MIL-STD-1553. BSEE required.
- **Electronics Packaging**—Requires knowledge of materials components design and fabrication. Shipboard, ASW, and EW experience helpful. Should have knowledge of printed circuit design, fabrication and application and some familiarity with stress dynamics and thermal analysis.
- **Electronics Engineer**—Requires a BSEE with 1-2 years ATE experience in circuit card testing. DTS-70 experience desirable.

LOGISTICS ENGINEERING

- **Reliability Engineers**—Position requires BSEE with 5 years experience in reliability engineering preferably on USN programs. Background should include thorough knowledge of MIL-HDBK-217D, MIL-STD-785B, and MIL-STD-756 to perform reliability predictions of electronic equipment, reliability programs, systems and equipment, reliability modeling and production.
- **Integrated Logistics Engineer**—BSEE or ME with 10+ years experience in Electronic ILS to include RFP response through program management.

INDUSTRIAL ENGINEERS

- **Senior Industrial Engineer (Methods)**—Experienced in any of the areas of Electronics, Machine Shop, Finishing or Bonding (composite and metal) in craft assembly or tooling. Classical Industrial Engineering skills required such as work simplification, manpower, forecasting, methods improvements, line balancing and short interval schedules. Experience required 4+ years. Requires BSIE.
- **Industrial Engineers (Standards)**—Several positions available in Standard Data Development using computerized "MOST." MILSTD 1567A compliance. Experience in manual or computerized "MOST" desired. Requires BSIE.

AEROMECHANICAL ENGINEERS

- **Mechanical Design Hydraulic Engineer**—BSME with 5+ years experience. Required to do elevator/crane design changes, testing, trouble-shooting and corrective action for in-house and field support. Familiar with DoD-D-1000.
- **Thermal/Gas Dynamicist**—5-7 years experience in gas dynamics and thermal analysis. Familiarity with finite difference thermal analysis, finite difference thermal codes and FORTRAN is also required. Supervisory or lead experience preferred.
- **Aircraft Stress Liaison**—BS in AE/CE/ME with 5-7 years experience in design and structural repairs of aircraft metallic and non-metallic structures. Familiarity with aircraft structures, specifications, manufacturing processes and procedures is also required. Strong background in classical hand analysis methods and hardware desirable. MRB authority experience.
- **Design Checkers**—Aerospace checkers experienced in all phases of design with good working knowledge of DoD-STD-100, ANSI specs and DoD-D-1000 specifications. Minimum requirements: BS or equivalent; 12-15 years experience.

SYSTEMS TEST ENGINEERS

- BSEE with a minimum of 5 years experience in test and troubleshoot of sophisticated military electronics equipment. This position requires a large percentage of travel to user location.

QUALITY ENGINEERS

- **Corrective Action**—Degree desirable with 3-5 years experience in the manufacture of military electronic or electromechanical assembly. Must be familiar with MIL-STD-1520 and MIL-Q-9858A. Background must include customer and supplier interface with MRB engineering experience.
- **Electromechanical Inspection**—BSME or BSEE degree with experience in analog and digital electronic technology, writing procedures and instructions.

SYSTEMS ENGINEERS

BS/MS/PhD EE/ME or related science with a minimum of 3 years experience in one or more of the following areas:

- Analysis of weapon system operational needs and concepts leading to design and integration requirements
- Analysis and trade studies to optimize performance parameters and define systems configurations
- Integration of technical parameters to assure interface compatibility
- Definition of combat system architecture
- Performance of functional allocation analysis
- Performance of electromagnetic compatibility analysis
- Performance of ASW analysis
- Technical control of communications systems, message processing and digital communications
- EW Systems Engineering

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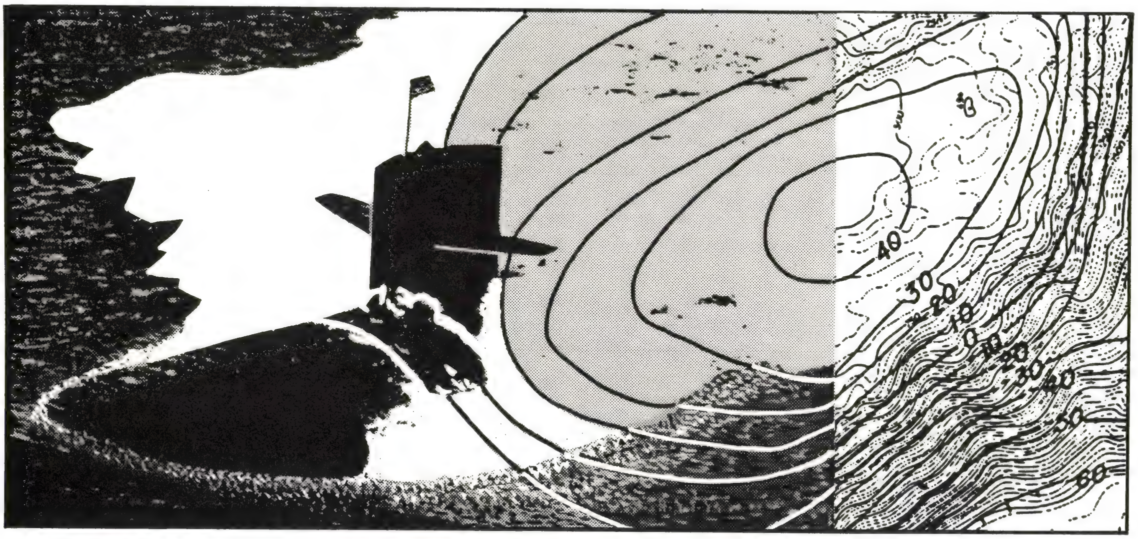

BELL AEROSPACE. WE'LL SURPRISE YOU.

We're in the forefront again, successfully creating highly sophisticated Gravity Sensing Systems for the Navy's most advanced navigation equipment. We've been there before, doing the "can't be done" without a lot of fanfare but with great success for over 50 years. We built the first American jet. We built the X-1 Rocket Plane, the first to break Mach I and fly at 126,000 feet. And, we built the X-2 that flew at 2,148 m.p.h. We built the Lunar Landing Training Vehicles. We built the first Post Boost Propulsion System. (It's still in service on the Minuteman Rocket). The list of Bell Aerospace firsts is a long one. After all, our business is technology.

We're still on the cutting edge, developing and perfecting Gravity Sensing Systems, working on High Energy Chemical Laser Systems and Beam Generators, leading the way in the development of Air Cushion, Amphibious Vehicles, creating a new generation of Liquid Propellant Thrusters. So, the next time someone asks, "Quick. Who did it first?" and the answer is Bell Aerospace, you may be surprised. But you should have known.

We're looking for people who can help us shape tomorrow's technology. Opportunities are exceptional for Engineers with a BS or MS degree and at least two years experience in one of the technical areas listed.

ELECTRONIC ENGINEERS

—Microwave RF, Antennas, Radar, Microprocessors, A/D Circuit Design, Control Systems, Signal Processing, Inertial Instruments.

PROGRAM MANAGERS

—Electronics

ELECTRONICS MARKETING MANAGER

SENIOR ILS ENGINEER

ELECTRONICS QUALITY MANAGER

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QUALITY CONTROL ENGINEERS

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ERIM REPORT #4

The Science of Range-Doppler Imaging

Fundamental range-Doppler radar imaging methods developed at ERIM are providing new capabilities in a variety of applications.

Range-Doppler Imaging

Fine Resolution microwave or laser images of objects which are rotating with respect to the radar system can be formed using the principles of range-Doppler imaging. Range resolution for such a system is provided by ranging with wideband waveforms subjected to pulse compression to accurately measure distance to the scatterers of interest. Cross-range, or azimuth, resolution is provided by performing Doppler-frequency spectral analysis (FFT) within range bins. Signals with higher Doppler frequency content are associated with scatterers of greater line-of-sight velocity which in turn implies increasing cross-range offset from object center. Display of the range bins and Doppler-frequency cells within range bins in a rectilinear grid results in a reflectivity image of the rotating object or scene.

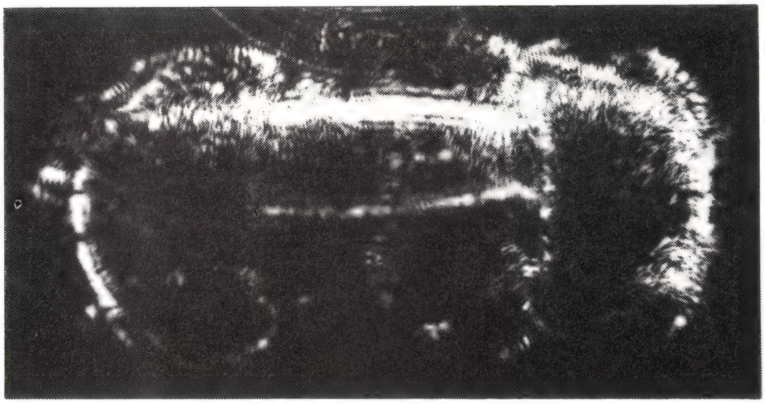
With this approach, finer azimuth resolution is obtained by performing the Doppler spectral analysis over increasing time intervals. However, as one strives for finer resolution the integration time can become so long that individual scatterers begin to move through the image resolution cells that one is attempting to form. In such a case the resultant image quality actually degrades with increased integration time.

Polar-Format Algorithm

A number of image-formation algorithms have been formulated to compensate for the effects of motion through cells during the integration period. The Polar-Format Algorithm, developed at ERIM for use with our ground-based and airborne imaging radar systems, has become widely noted as an extremely powerful, yet elegantly simple and efficient method for overcoming these previous limits of imaging capability. The images below show a Volkswagon and its associated microwave range-Doppler image processed using the Polar-Format algorithm. This image was produced using the ERIM ground-based, range-Doppler imaging facility.

Applications

Fine-resolution range-Doppler imaging is applicable to a number of situations, including space object imaging (SOI), Inverse Synthetic Aperture Radar (ISAR), and Spotlight-mode SAR for airborne imaging of ground scenes. In principle, the approach is suited to both optical and radar wavelengths, Also, the theory has been extended to allow for three-dimensional imaging of objects given suitable signal collection configurations.



The Environmental Research Institute of Michigan (ERIM) is a scientific research institute that performs contract research services for a variety of sponsors. Our sponsors include government organizations, industry, and universities. Research at ERIM focuses upon remote sensing systems, devices, and techniques that span the electromagnetic spectrum. Within this broad research area, staff members employ their knowledge of modern electronics, optics, computer science, and infrared and microwave physics.

Career Opportunities

ERIM's technical divisions have research and management positions available in Ann Arbor, MI, Washington, DC, and Los Angeles, CA. Positions are available at several levels in the following areas:

- **Radar System Engineering and Analysis**
- **Signal and Image Processing**
- **Microwave Scattering and Measurement Engineering**
- **Diffractive Optics**
- **E-O/IR System Design and Analysis**
- **Infrared Phenomenology**
- **Computer Vision**
- **Optical Computer Systems**
- **Phase Retrieval/Signal Reconstruction**

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- Digital signal processing, modulation and coding

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- Spread Spectrum ESM/ ECCM/ECM
- Signal detection and estimation
- Optical processing
- Antijam systems

Advanced Technology
- Signal processing, artificial intelligence
- GaAs devices
- Heterojunction device physics
- Network analysis
- Signal detection theory
- Covert transmissions

Software Engineering
- Communication software
- Scientific, real time programming
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LEAD SYSTEMS ENGINEERS: Responsible for directing system-level effort in installing and operating test computer and leading the integration with the fuel system management set. BS/MSEE or CS and 10 years experience working with large computers in a military environment required.

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- PROGRAM SCHEDULERS
- SOFTWARE TEST ENGINEERS
- SUPERVISORS
- LEAD DISPLAY ENGINEERS
- SOFTWARE SYSTEMS ENGINEERS
- MECHANICAL (Packaging) ENGINEERS
- SR. ELECTRICAL (Design) ENGINEERS
- MANUFACTURING TEST ENGINEERS
- MANUFACTURING (PCB) ENGINEERS
- INDUSTRIAL ENGINEERS
- SOFTWARE & HARDWARE CONFIGURATION MANAGEMENT ENGINEERS
- SOFTWARE (Real-Time Design) ENGINEERS
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We offer highly competitive compensation and excellent benefits including a liberal relocation allowance. For consideration, please send resume and salary history to: **Gary Van Arsdale, Human Resources Department EDN, Simmonds Precision Instrument Systems Division, Panton Road, Vergennes, Vermont 05491.** Affirmative action/Equal opportunity employer. U.S. citizenship is required.

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Parts Specialists Engineers

Must be familiar with MIL and High Rel specifications such as MIL-STD-883, MIL-STD-38510, MIL-S-19500 and skilled in application and derating, screening tests, parts degradation, and evaluation of failure analysis.

Parts Management Engineers

Requires familiarity with the management of a parts space program for either NASA or DOD projects, including the generation and/or review of Parts Program Plans. Must also be familiar with MIL and High Rel specifications and capable of controlling and/or justifying non-standard parts applications for both in house designs and subcontractors. Knowledge of MIL-STD-975 and MIL-STD-1546/1547 desired.

Interested qualified candidates are asked to send both resume and salary requirements in confidence to: C. Gakeler, **RCA Astro-Electronics**, Dept. 465327, P.O. Box 800, Princeton, NJ 08543-0800.

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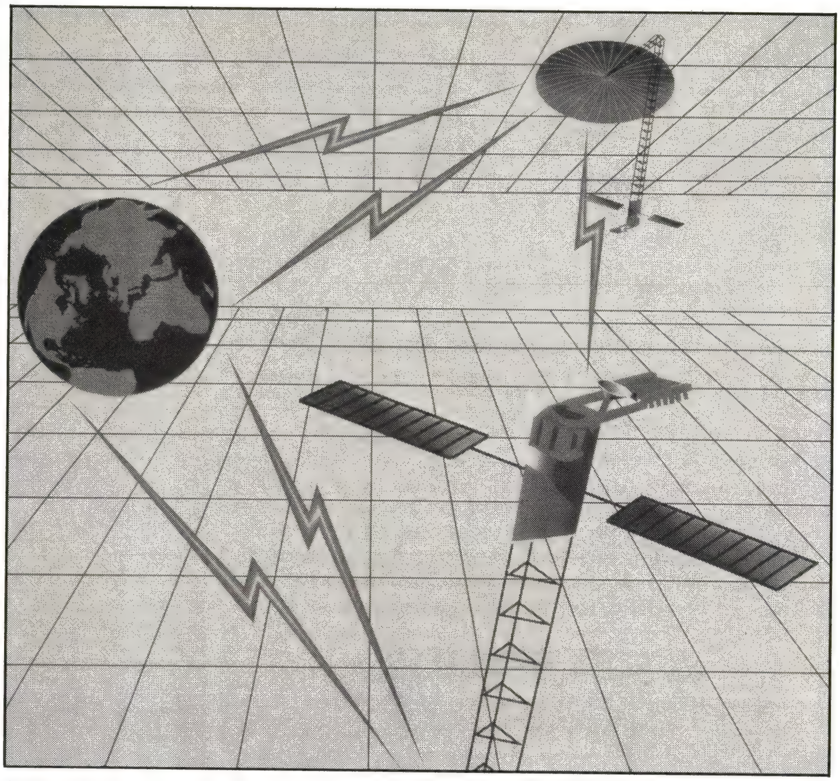

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Abbott Transistor Labs Inc 108
Acculex Corp 257
ADPI 259
Advanced Microcomputer Systems Inc 261
AEG Corp 269
AIE Magnetics 257
Airpax Corp/Frederick Div 46
Aluminum Filter Co 229
AMCC/Applied Micro Circuits Corp 26-27
AMP Inc 149
Amphenol Products, An Allied Co 182
Aptos Systems Corp 79
Arnold Magnetics Corp 166
Ault Inc 150
Autodesk 192
Belden Electronic Wire & Cable C4
Bering Industries Inc 94
Boeing Electronics Co 93
B P Microsystems 260
Cahners Exposition Group 107
California Devices Inc 189
California Scientific Software 258
Calmos Systems Inc 121
Carroll Touch 88
Casio Inc 86
Cermetek Microelectronics Inc 261
Chartered Electronics Industries/ Singapore Tech Inc** 144D
Chomerics Inc 98
Circuit Technology Inc 209
C&K Components Inc 6
Comlinear Corp 87
Computer Products Inc 247
Connecticut microComputer Inc 260
Crystek Microelectronics 259
Cybernetic Micro Systems 30
Cypress Semiconductor 74
Dash, Straus, and Goodhue 92
Datel 190
Densitron 257
Dibble Electronics Inc 258
Digital Technology Inc 68
Displex Inc 258
Dow Corning Corp 23
Duracell Inc 123
DY-4 Systems 258
EF Johnson Co 220
E G & G Almond Instruments 40
Elcon Products International 261
Electro Mechanical Systems Inc 208
Electronic Designs Inc 202-203
Electronic Modular Systems Inc 273
Electronic Solutions 61
Emcor Products 271
Emulation Technology Inc 261
Endicott Research Group Inc 162
Engineering Information Services 48-49
Epoxy Technology Inc 234
Equipto Electronics Corp 269
E-T-A Circuit Breakers 258
Factron Schlumberger** 250-251
Fairchild Communications 233
Fairchild Semiconductor Corp 65
Faraday Electronics 215
Feller AG 231
Ferro-ECA Electronics Co 218
Force Computers Inc 28-29
Fujitsu America Inc/ Storage Products 207
Fujitsu Microelectronics Inc* 44-45
FutureNet/Div of Data I/O 84-85
GE/Intersil C2
General Connector Corp 238
General Electric Semiconductor Products 14-15
Glassman High Voltage Inc 204
Gould Computer Systems Div 219
Grayhill Inc 212
Harris Semiconductor 135, 137, 139
hawa 205
Heurikon Corp 276
Hewlett-Packard Co 12-13, 243-244
Hi-G Co 216
Honeywell Digital Products Center 212
Honeywell Signal Processing Technologies 237, 239, 241
Honeywell Test Instrument Div 10
Humphrey Inc 138
Hyundai Semiconductor 92
Industrial Electronic Engineers Inc 154
Inland Motor 124
Inmos Corp 11, 33
Integrated Circuits Inc 260
Integrated Device Technology 210
Integrated Power Semiconductors 254-255
Intel Corp* 110-111
Intel Corp 152-153
Introl Corp 259
Ironwood 260
John Fluke Manufacturing Co Inc 76, 259
Jonathan Mfg Co 211
Kepco Inc 99-106
Key Tronic 213
KMW Systems Corp 73
Laserpath 230
Ledex Inc 227
Linear Technology Corp 195
Litton Electron Devices 156
Lockhart Industries Inc 246
Loctite Corp 141
MathSoft 268
Matrox Electronic Systems Ltd 274
McDonnell Douglas 142
MCG Electronics Inc 162
McLean Engineering 225
Measurement Systems Inc 277
Micron Technology Inc 222
Mini-Circuits Laboratories 3, 4, 24-25, 187
Molex Inc 308
Monolithic Memories Inc 16-17
Motorola Components Div 223
Motorola Semiconductor Products Inc 181
M S Kennedy Corp 143
MuShield/Bomco 223
NCR Microelectronics Div 21
New Micro 177
North Atlantic Industries Inc 38
Oasys/Div of XEL 125
Omation Inc 261
Omnibyte Corp 163
Optimal Technology 257
Orbit Semiconductor Inc 228
OrCAD Systems Corp 258
Performance Semiconductor Corp 41
Permag Corp 227
Philips Elcoma Div** 42-43, 122B-C
Philips Test & Measuring Instruments Inc** 122A, 144C
Pioneer Standard Electronics Inc 97
Plessey Microsystems Ltd 263
Plessey Semiconductors 50-51
Polyphase Instrument Co 260
Potter & Brumfield 95
Powercube Corp 245
Precision Filters Inc 236
Precision Monolithics Inc 173
Prototek Inc 259
Qua Tech Inc 257
Raytheon Semiconductor Div 57
RCA Solid State Div 36-37
Rifa 224
Rifa** 253
Rockwell International 265
Samtec Inc 260
Sangamo Westson 258
Seagate Technology 52
Servometer Corp 221
Shelly Associates 259
Siemens AG** 110-111, 122D, 144A
Signetics Corp* 42-43
Siliconix Inc 69-71, 197
Silicon Systems Inc 66, 67
Sorensen Co 201
Spectrum Software 39
Sprague Electric Co 31, 63, 119
Sprague-Goodman Electronics Inc 261
Stag Microsystems Inc 18
Stevens Products Inc 257
Sumitronics Inc 32
Sunrise Electronics Inc 252
TDK Corp 176
Teac Corp** 144B
Technitrol Inc 196
Tektronix-CAE Systems 164-165
Tektronix Inc 8, 34-35, 144, 178-179
Teledyne Crystalonics 266
Teledyne Relays 140
Teledyne Solid State Products 261
Thaler Corp 264
Thomson Components-Mostek Corp 80-81, 82-83
Thomson Semiconductors** 44-45
Titan/Sesco 151, 242
Torin Corp 155
Toshiba America Inc 69, 198-199
Total Systems Integration 259
Transmagnetics Inc 150
TRW Electronic Components Group 234

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AD INDEX

TRW Resistive Products Div 235
Uniform Tubes Inc 68
Union Carbide Corp/
  Electronics Div 54
United Technologies Microelectronics
  Center 126
Universal Data Systems C3
Valpey-Fisher/Matec Corp 262
Vernitech 259
Vicor Corp 180
Video Monitors Inc 214
Visionics Corp 258
VTC Inc 90-91, 221, 225, 229
Whitesmiths Ltd 175
WinSystems Inc 258
Wintek Corp 260, 261
Zilog 72

Recruitment Advertising

Bell Aerospace 299
Boeing 282
Comarco Weapons Center 290
Eaton Corp 290
Erim 300
E-Systems Garland 297
Fairchild Weston Systems 280
Garrett Turbine Engine Co 288
General Dynamics Data 295
General Dynamics Pomona 293
Grumman Recruitment 281
GTE Government System 286
Kollsman Instrument 285
Lear Seigler Astronics 291
Lockheed Sunnyvale 303
M/A Comm 280
Martin Marietta, Baltimore
  Aerospace 298
Micro-Dynamics Inc 296
Microwave Power Devices 302
Motorola Government
  Electronics 294
MPC Products Corp 302
MTI 296
Raytheon Missile Systems 284
RCA Astroelectronics 302
Riker Personnel 302
Siemens Corp 287
Simmonds Precision 302
Singer, HRB 292
Sperry 301
Sperry Systems Management 289
Texas Instruments 283
Wallach Associates 296

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

Semicustom linear IC market to be worth $360M by 1990

Advances in design automation will be a major factor in the expected boom of the market for semicustom linear ICs through the remainder of the decade, according to HTE Management Inc, a Scotts Valley, CA, market-research and consulting company that specializes in the semiconductor industry. In 1985, the market was valued at $72.8 million—14% of the total market for custom linear and digital-linear ICs —and by 1990, semicustom linear ICs should be worth $360 million in sales. HTE expects that figure to be 21.5% of 1990 sales in the larger category.

This growth will track the ability of computer-aided design (CAD) systems to handle linear components. "CAD has been a big stumbling block," says HTE founder Steve Z Szirom. "Now, almost-automated gate-array design systems have become realities; tomorrow, the technology will be fully automated, available on relatively low-cost workstations, and [it will] be able to provide pure digital, pure linear, or a mixture of digital and linear functions on the same chip."

Another factor pushing market growth is the entry of several large companies as well as start-ups financed by venture-capital companies. Twenty-one companies are attempting to manufacture and sell semicustom linear ICs, up sharply from a few years ago. On the other hand, the market could be limited by designers' tendency to render traditionally linear functions in digital circuitry.

HTE sees bipolar technology as the process most often used to create semicustom linear ICs. "CMOS will certainly make inroads," says Szirom, "but not at the rate we see in digital. Bipolar processing is needed to build [high-performance] devices, such as wideband amplifiers with high slew rates. CMOS linear semicustom is the candidate of choice for mixed-process products."

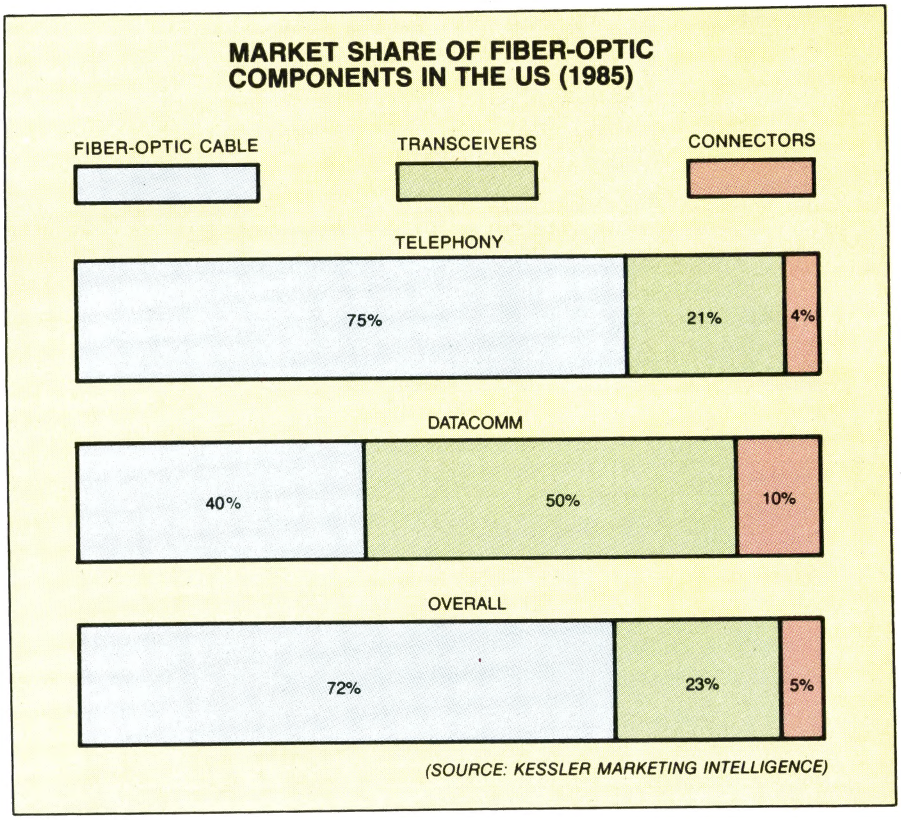
Datacomm systems to use $1B of F-O equipment by 1995

Data-communications applications will be the driving force behind growth in the market for fiber-optic equipment, according to Kessler Marketing Intelligence, a research firm based in Newport, RI. Datacomm systems will use more than $1 billion worth of fiber-optic cables, transceivers, and connectors in 1995, up from $120 million in 1985.

In datacomm applications, more capital outlays are devoted to transmitters and receivers than to cables or connectors. Datacomm networks tend to connect a high number of workstations and computers over shorter distances than do telephone networks. Telephony applications demand great lengths of fiber-optic cable, typically for high-capacity, long-distance phone lines—for example, in the Northeast Corridor of the United States.

The researchers also compare the markets for single- and multimode fibers. About 75% of the fiber-optic cables used in all applications employ single-mode fibers. The chief use is in telephony, which can more easily bear the cost of the expensive laser light sources used with single-mode fiber. Yet the use of multimode fiber is also growing; purchases of multimode-fiber cables (measured in kilometers) will increase from 1985's 227,800 km to 1,000,000 km in 1991.

Multimode-based systems use LED light sources, which are less expensive than lasers. The cost of laser manufacturing is falling, however, and companies are developing high-powered LEDs for single-mode systems, so designers of both datacomm and telecomm systems will have a wider variety of choices.



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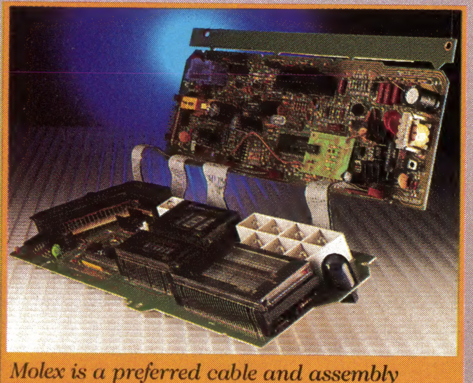

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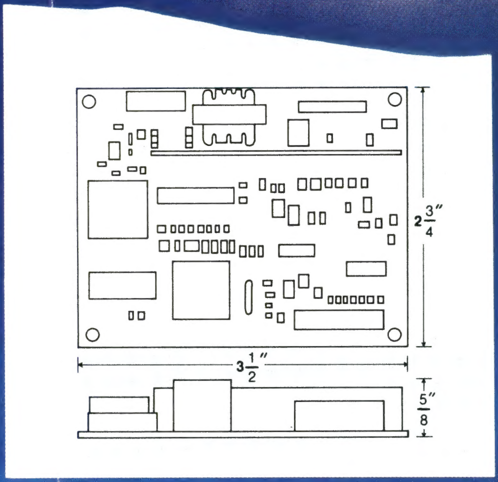

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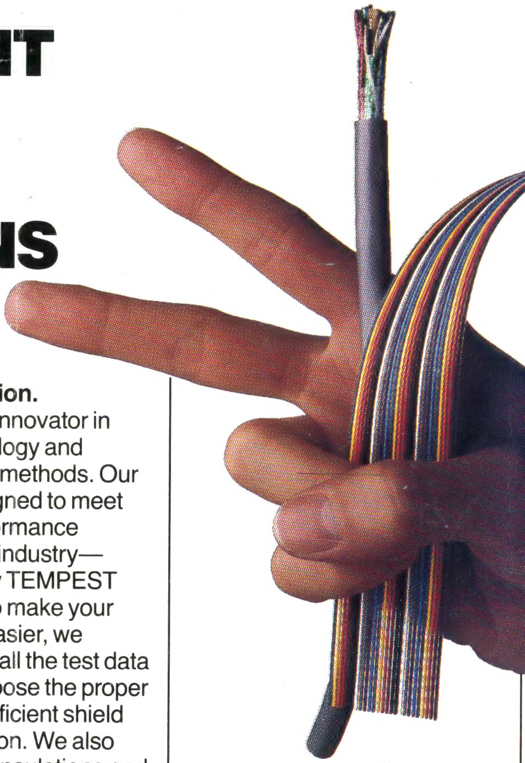

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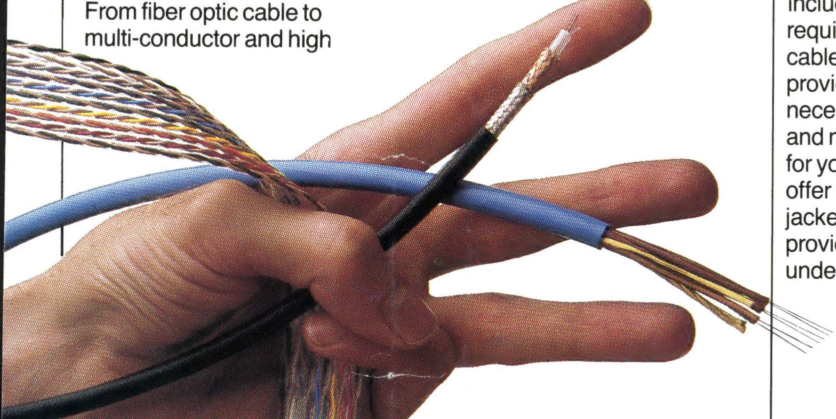

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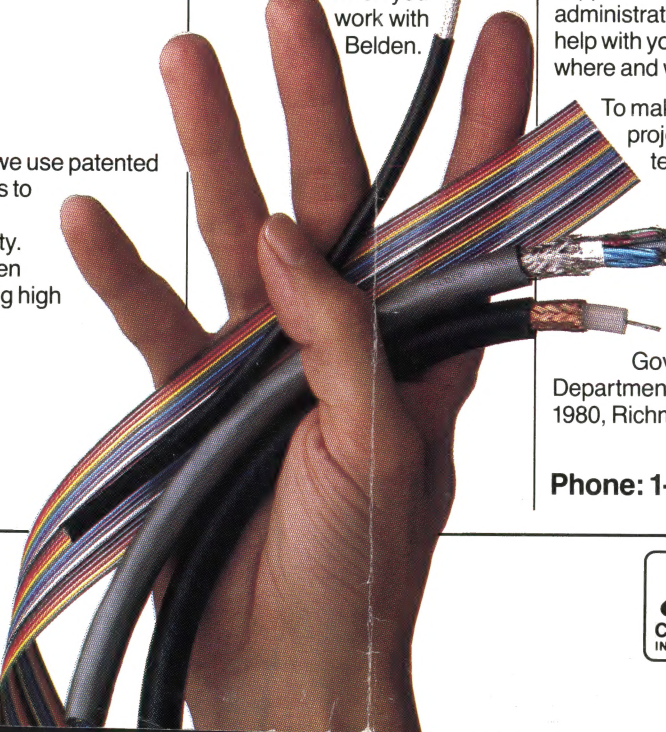

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